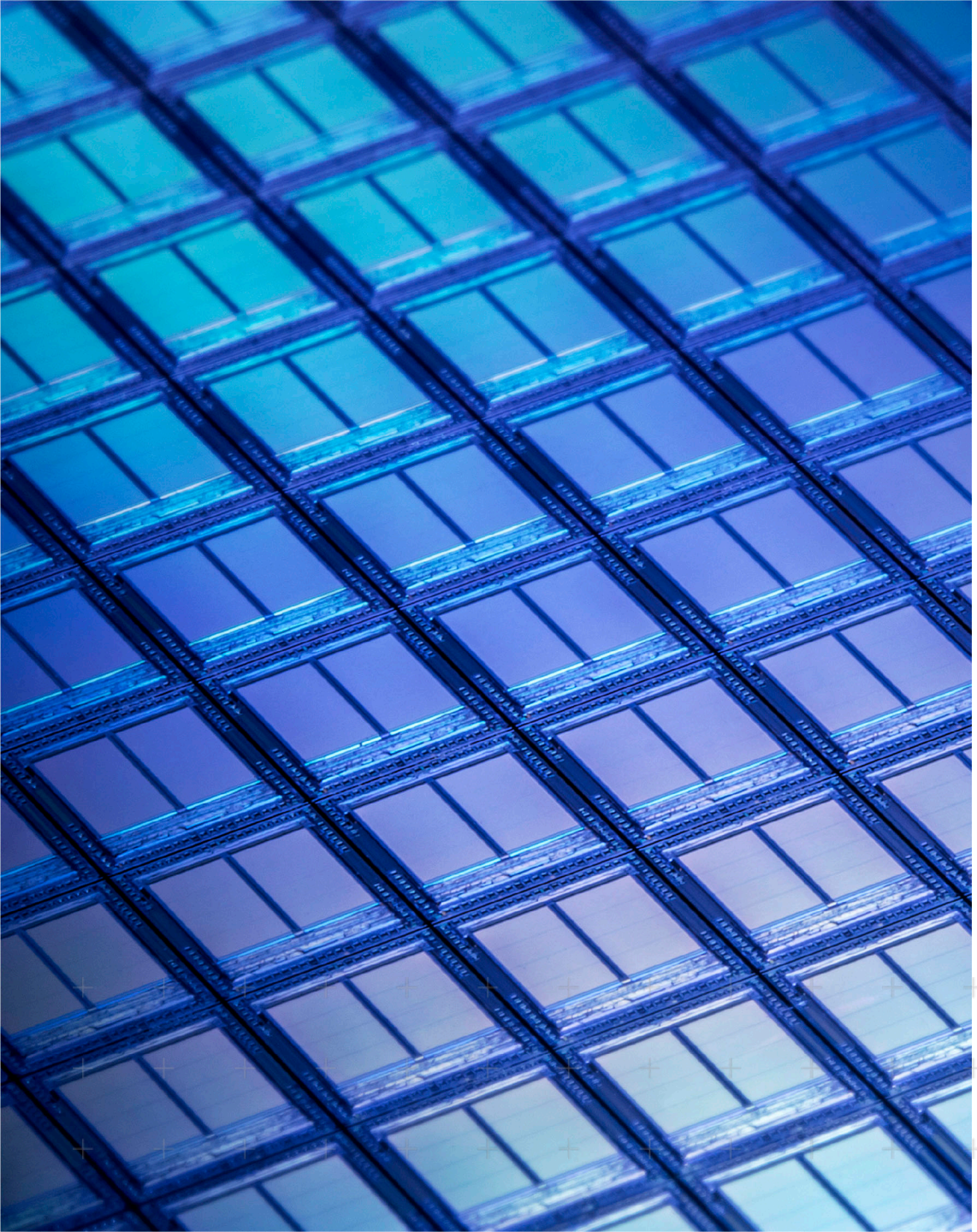


Plasma Dicing “The Next Normal”

Richard Barnett

Senior Product Manager – Etch

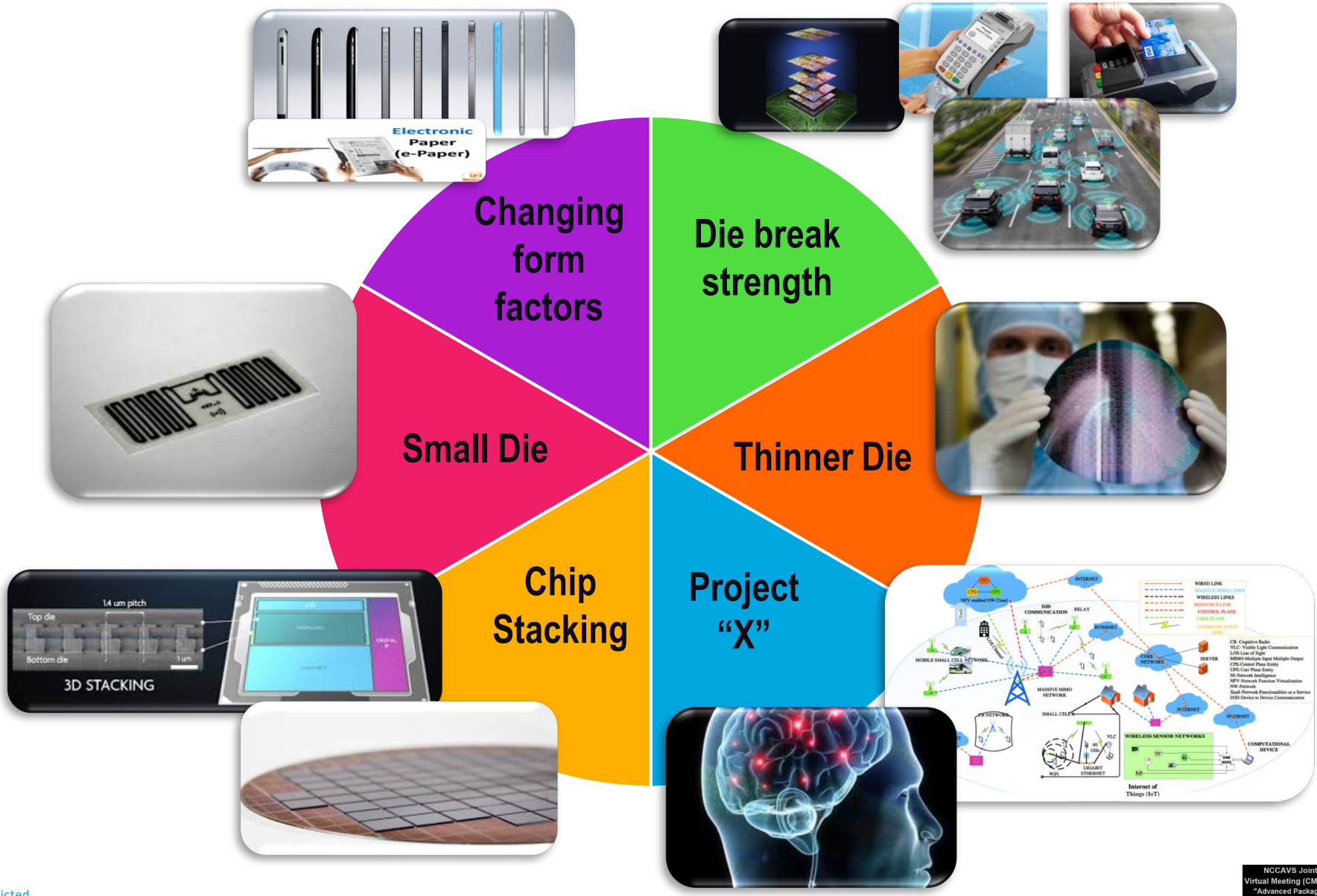
NCCAVS Joint Users Group
Virtual Meeting (CMPUG, PAG, TFUG)
"Advanced Packaging Technology"
June 10, 2020

10th June 2020

Content

- Device trends & how they relate to wafer singulation
- Benefits of plasma dicing
- Integration is Key
- SiP
- Examples of Implementation
- Summary
- Q&A

Device Trends – Distributed; Mobile; SiP; At the point of interaction;…..



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Benefits of Plasma Dicing

No Damage

- Chemical etch
- No chips, cracks
- No particles
- Controlled sidewall
- No heat zones in Si
- High Etch Rates
- Parallel Process
- Thin Wafers <50µm

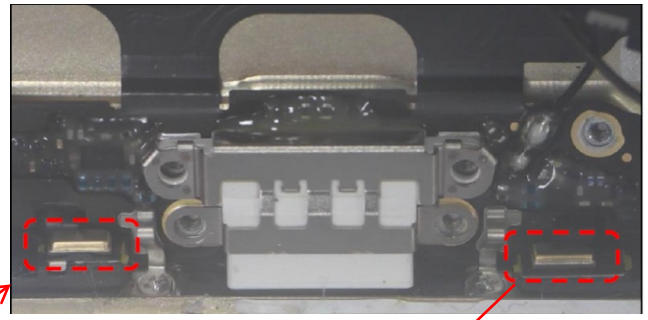
Flexible Layouts

- Kerfs <10µm
- Non-orthogonal
- No EE
- Free die shape
- Great for MPW

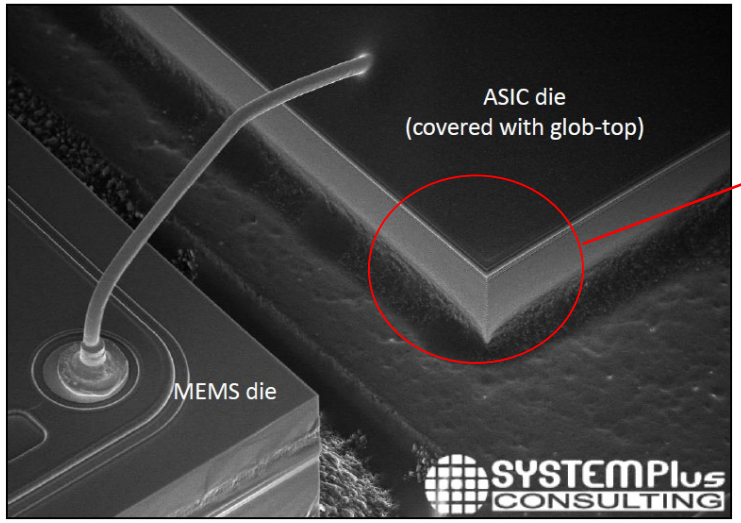
"Front-End" for the "Back-End"

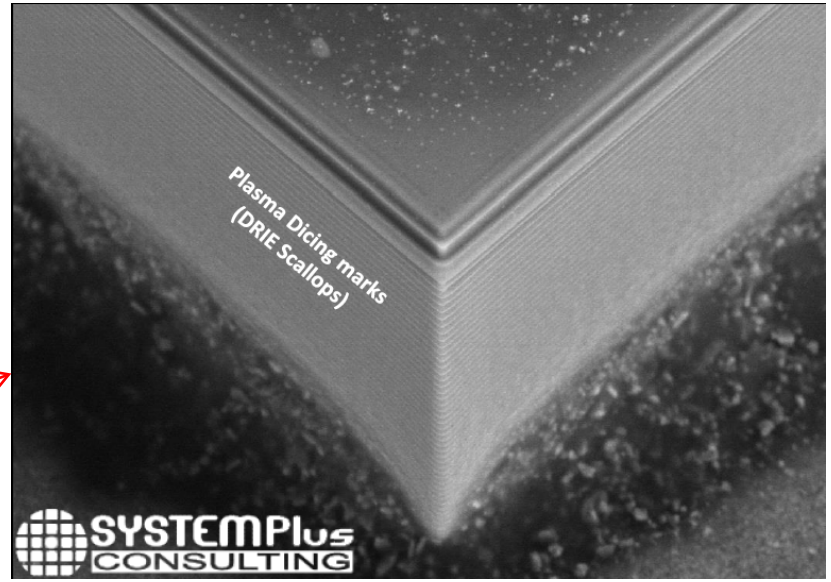
- Clean process
- Process control
- Endpoint
- Wafer Monitoring
- No consumables
- Repeatable
- Consistent
- Cluster platforms

Plasma Dicing already in iPhones



Knowles microphone

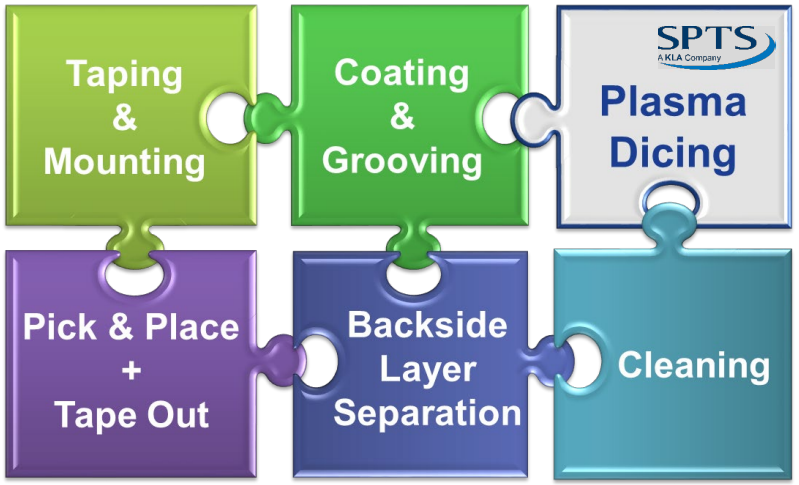




Microphone by Tier#1 IDM
ASIC by European Foundry
Dicing by SPTS Rapier PM

Integration is Key

- "Whole Flow" approach established as "Best Practice"

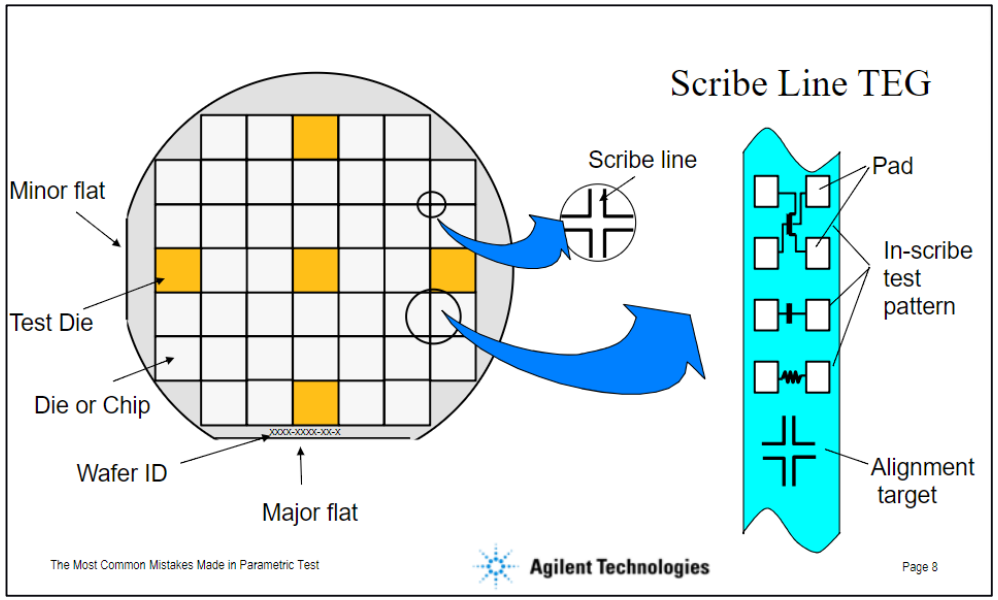


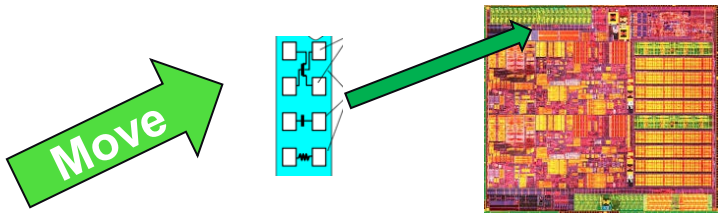
- Collaborations & co-working across back-end community
  - LASER Grooving/Coatings OR Design for Plasma Dicing
  - Tapes
  - Dry Strip or Wet Chemistries
  - Backside Layer Treatment
- Plasma Dicing cannot be treated in isolation

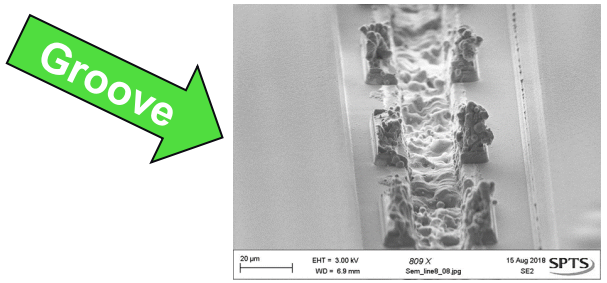
Dicing Highways

Busier than lanes

- Key demand
  - **We need compatible & defined features to etch**
- Dicing Lanes are not empty !
  - Metals & Dielectrics – not wholly compatible with plasma DAG
- Options for management of TEGs
  - **“Move or Groove”**



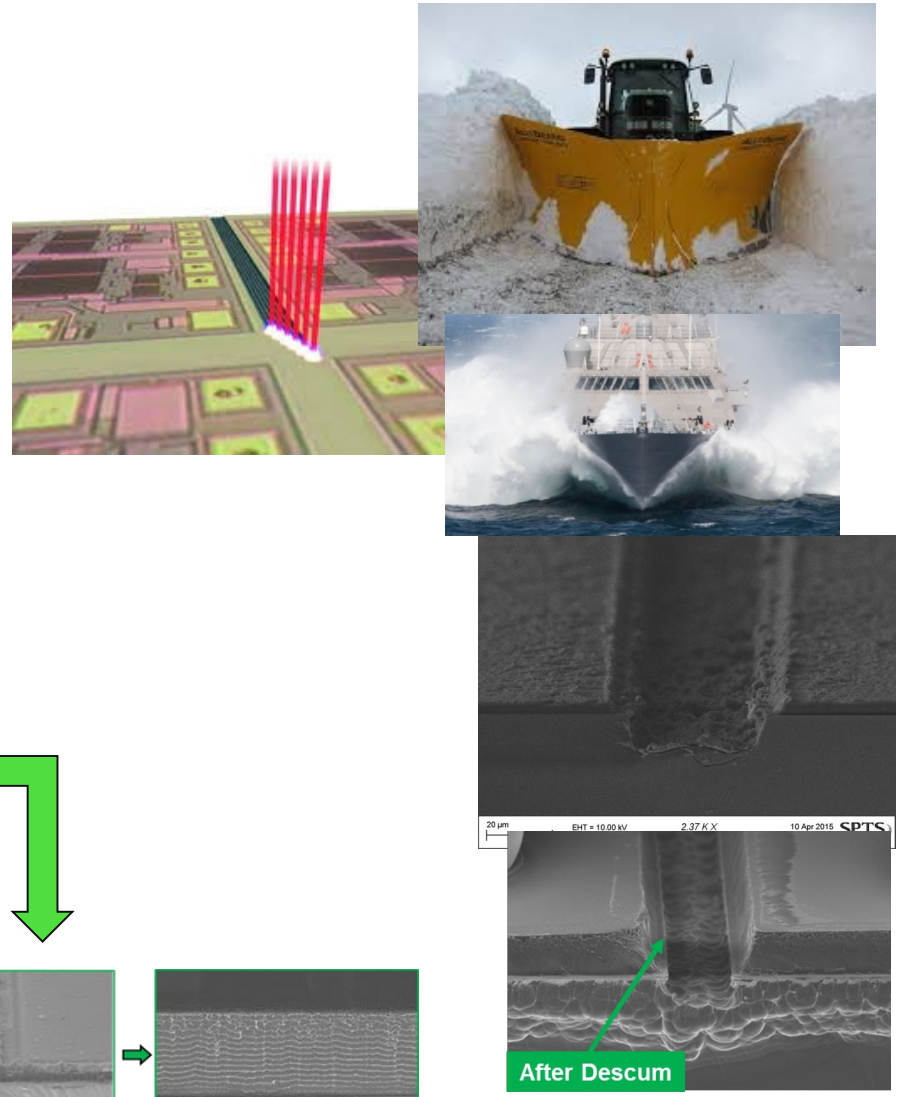




Integration

“Grooving”

- LASER Grooving has become a popular approach
  - Requires coating to protect die, define lanes
  - Not a catch-all solution
- Coating selection is important
  - Selective to etch chemistry
  - Post-etch removal
- LASER clears lanes, but there can be side effects
  - Recast, snow-plough, bow-wave
- Sympathetic process tuning required
  - Good Groove = Good Singulation
  - Use etch conditions to remove residues from Si surface
  - “Descum” – just as we do in the compound world

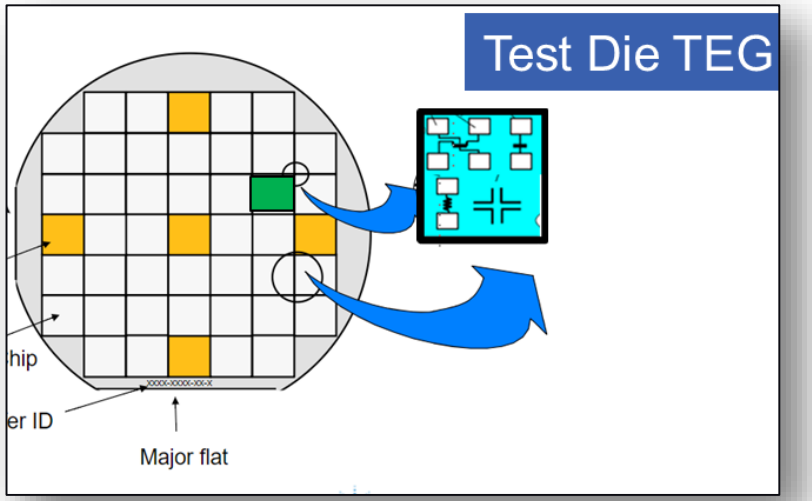


Process integration is critical, hardware integration is not

Integration

“Moving”

- Consider Backend (BE) at the start of design process
  - Narrow lanes can release real estate; die layout & shapes
  - Narrow lanes cannot host TEGs
  - TEG Die to accommodate for test structures, alignment marks can solve this



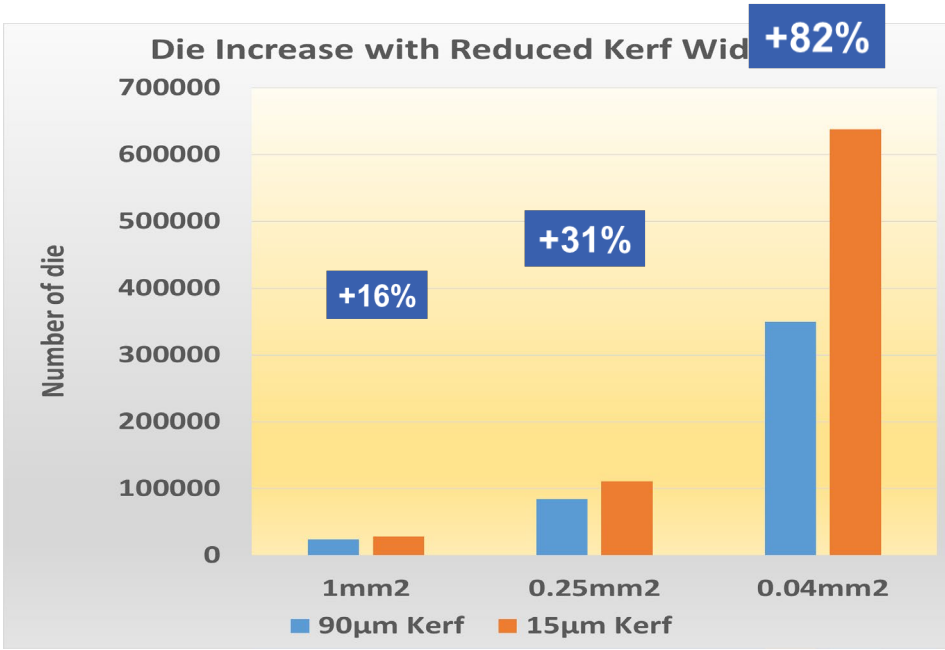
- Designers will need to know if product will be plasma diced
  - Process flow architecture to accommodate shift TEG Die

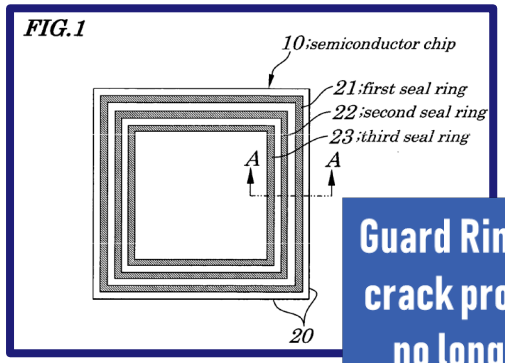
Design for Manufacture & Test is required

Wafer Layout Gains

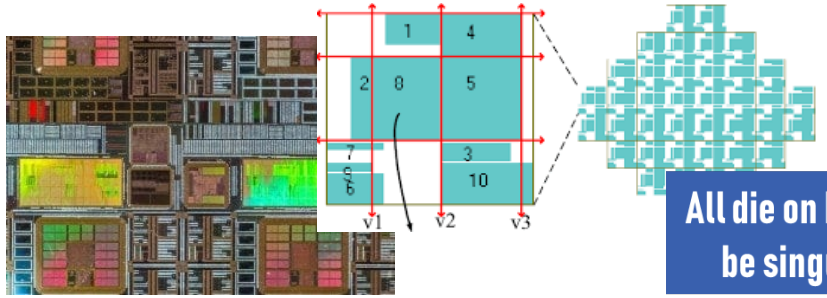
Increasing die per wafer/reducing costs

- Narrower kerfs can be realised using Plasma Etch
  - <10µm
- More real estate for die
  - Guard Rings/Seal Rings can be shrunk/removed
- Inexpensive approach to increasing “fab capacity”
  - Reduce wafer costs
  - Reduce fab costs
- Multi-product Wafers
  - Where ALL die can be used





Guard Rings to prevent crack propagation are no longer required



All die on MPW can be singulated

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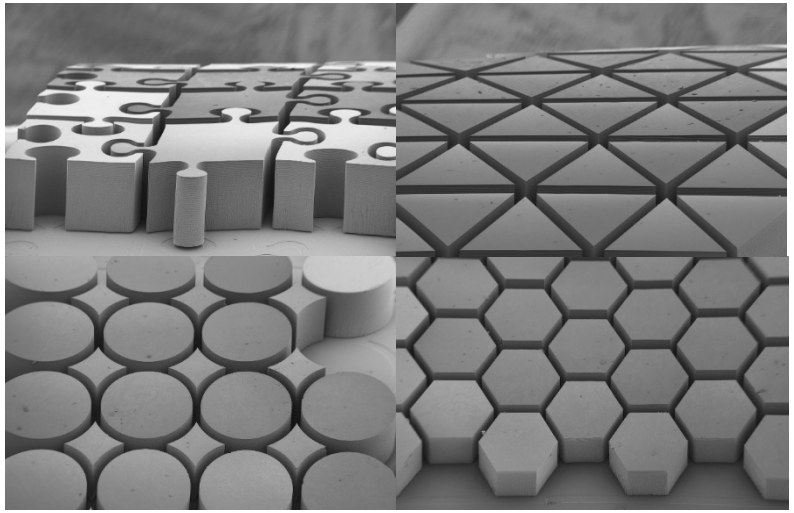
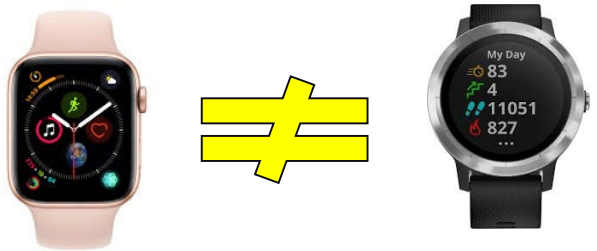
Form factor flexibility

- SiP allows minimised footprint for increased functionality
  - But design rules require minimum separation between die; 60µm
- Novel solutions may be required for best packing density

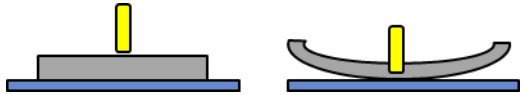


Examples of plasma diced structures
Mosaic & Rapier-S

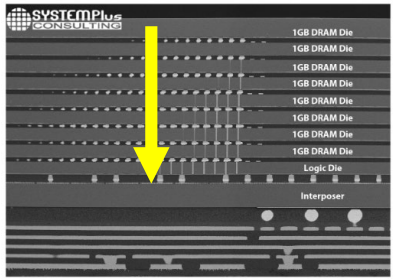


- Designers are able to take advantage of PD benefits
  - For both Product & Device

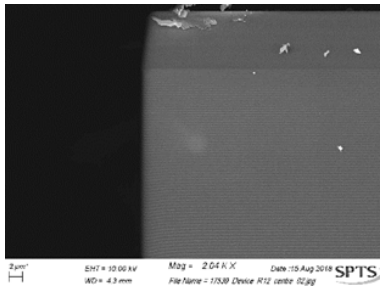
SiP Drivers for Plasma Dicing

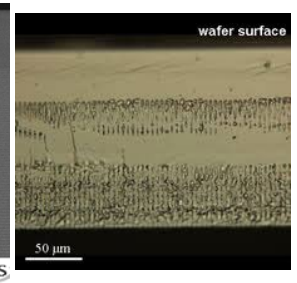


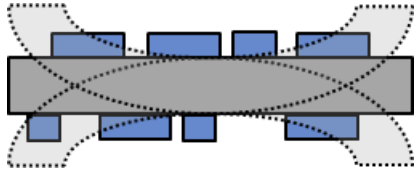
- Thinner Wafers
  - Singulation method critical to ensure no risk of in-service failure
- Stacked die
  - Pressures on die from stack stresses
  - Prevent particles from interfering with bonding; functionality
- Improving Yield at Singulation
  - Mechanical
  - Inspection
- Double sided SiP
  - Higher *Front **and** Back die strength* needed for dual plane deformation
- Automotive Reliability
  - ISO26262
  - Critical devices for ADAS need to cope with impacts, vibrations, etc



AMD Radeon Vega HBM2 Cross-Section







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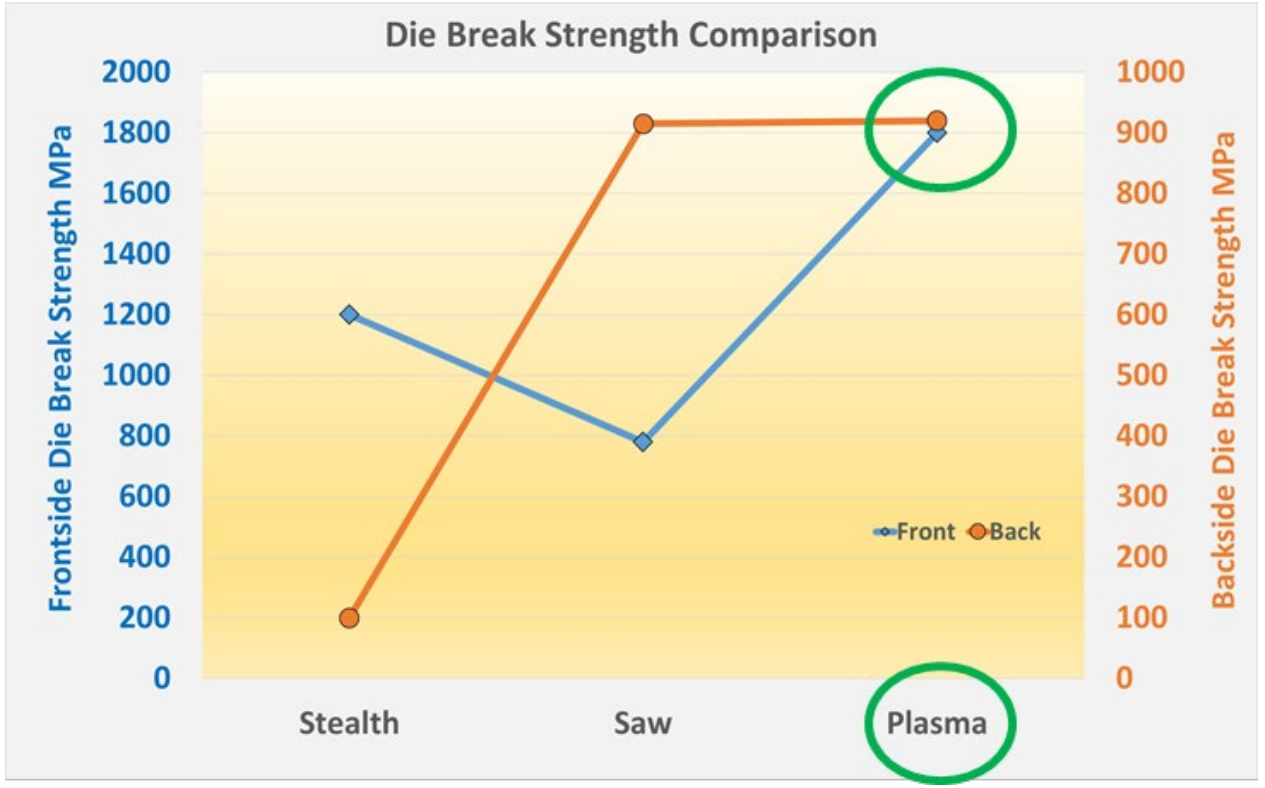
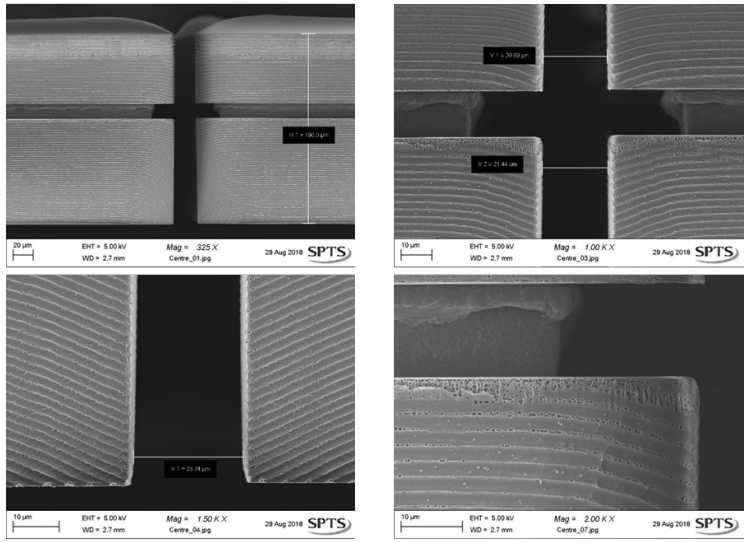
Achieving higher die break strength

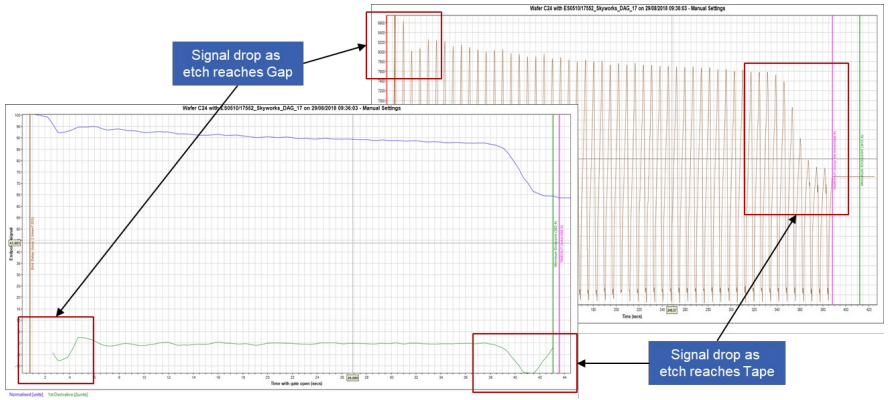


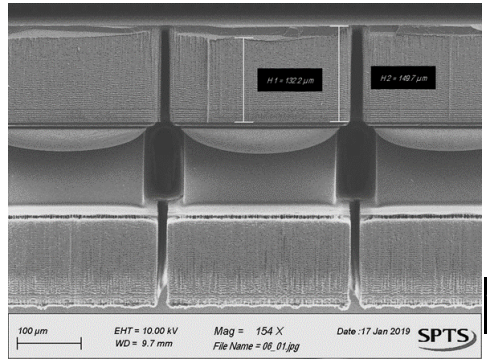
- **No sidewall damage** at all due to chemical etch
- Preventing undercut (at tape) protects die strength gain
- Plasma is only method to improve front & back side strength

Filter Devices

- Small die size of filters (BAW) make them ideal candidates for plasma dicing
  - More filters being utilised in newer mobile phones
  - Increased die per wafer improves cost scenarios
- Filters are typically bonded wafer pairs
  - Plasma singulating stack of wafers
  - Avoids costly and time consuming individual die bonding
- Plasma etch through a void between wafers
  - Key is to manage protection of “exposed” Si during void transition
  - Examples shown with no impact on this region
  - Claritas can even detect when etch front traverses the void region
- DAG or DBG?
  - Both can be utilised for stacked wafers







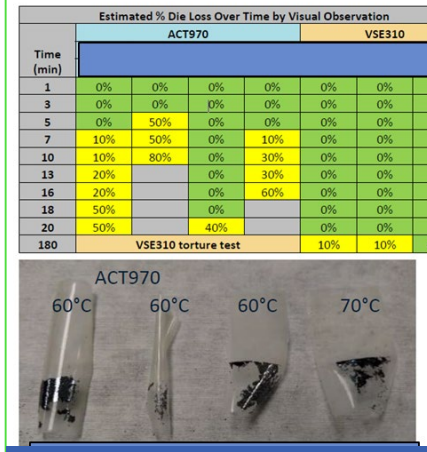
Defluorination & Strip

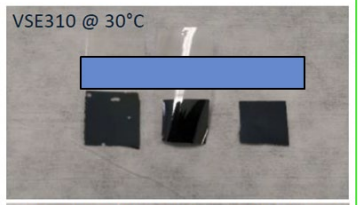
- To remove F and residual mask material
- LASER Coatings
  - Rinse off in DI H_2O
  - Plasma has **no impact** on solubility
- PR/Polymer
  - Wet…
    - Standard wet cleans can attack the tape
    - Versum → chemicals with no tape attack & no die loss
  - Dry…
    - O_2 dry strip with additional step to assist with F residue reduction
    - Reduces F levels to < control levels

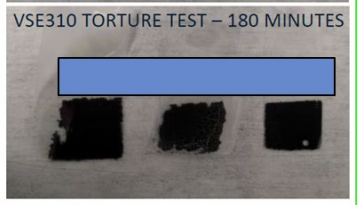
VERSUM MATERIALS

TAPE COMPATIBILITY SUMMARY

Estimated % Die Loss Over Time by Visual Observation							
Time (min)	ACT970				VSE310		
1	0%	0%	0%	0%	0%	0%	0%
3	0%	0%	0%	0%	0%	0%	0%
5	0%	50%	0%	0%	0%	0%	0%
7	10%	50%	0%	10%	0%	0%	0%
10	10%	80%	0%	30%	0%	0%	0%
13	20%		0%	30%	0%	0%	0%
16	20%		0%	60%	0%	0%	0%
18	50%		0%		0%	0%	0%
20	50%		40%		0%	0%	0%
180	VSE310 torture test				10%	10%	<10%

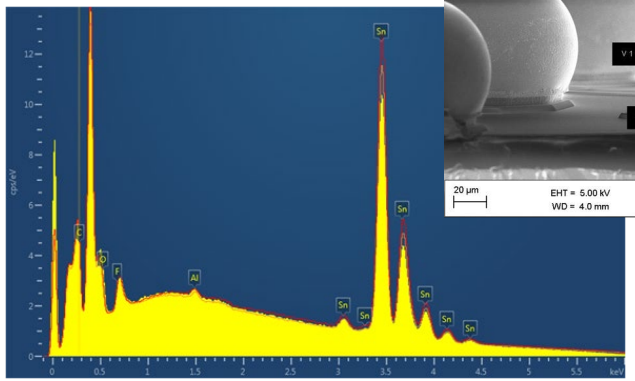


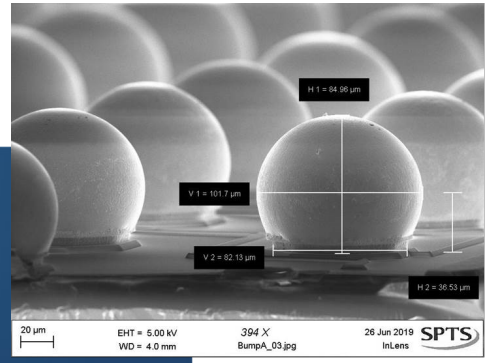




SIGNIFICANTLY LESS TAPE DEFORMATION AND DIE LOSS WAS SEEN WITH VSE310

Joint paper at Semicon Europa 2018





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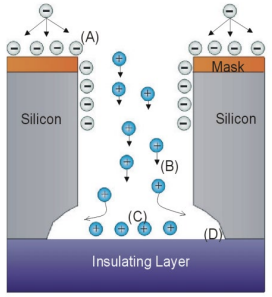
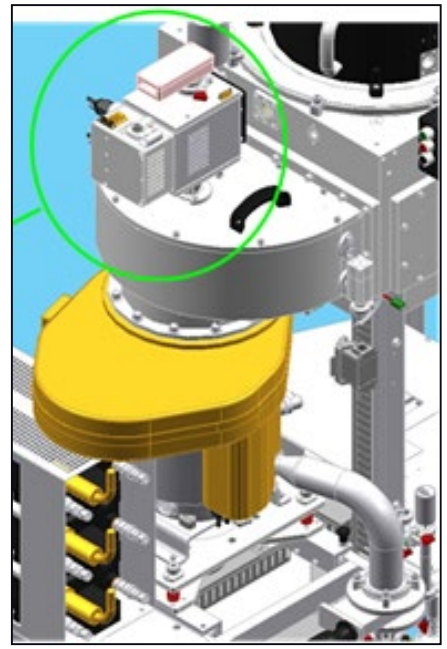
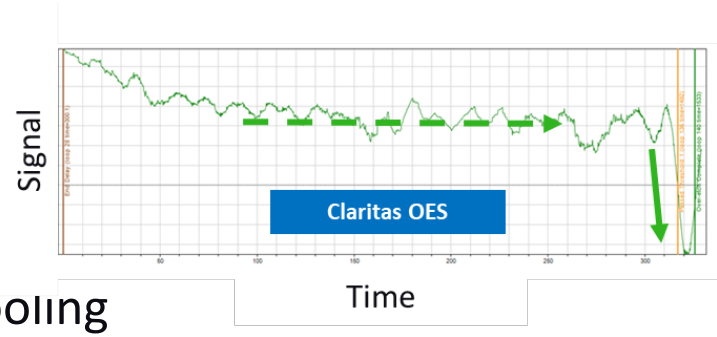
Safe-guarding High Value Wafers

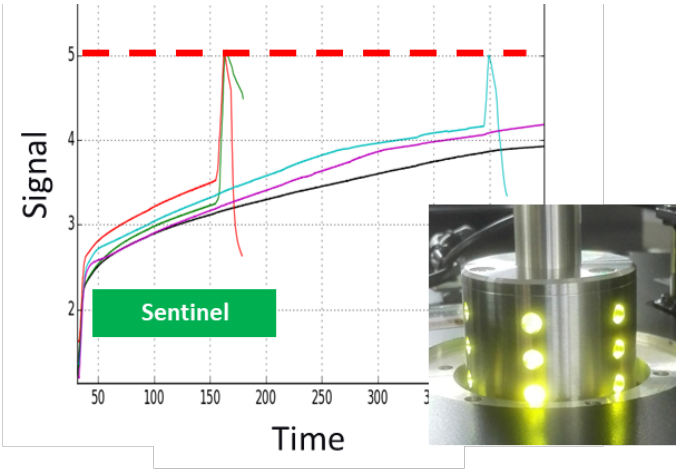
- Claritas end-point detection
  - Sensitive OES EPD (<0.05% OA; >100mT process pressures)
  - Minimal over-etching; Maximises throughput
  - Minimises notching
  - → Maximises die strength







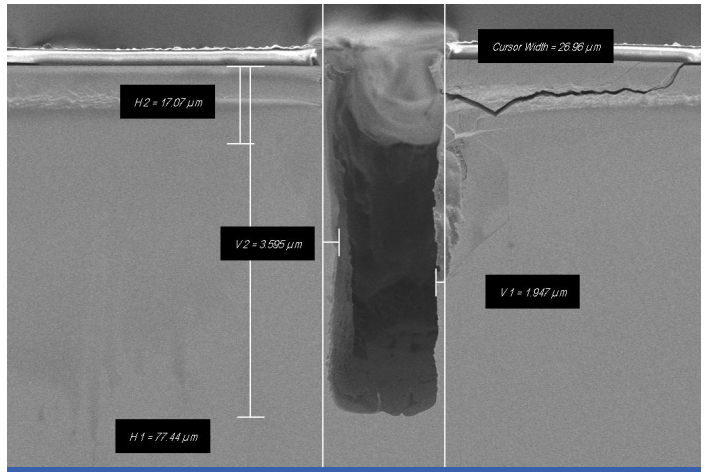
- Sentinel™ monitors substrate & alerts for loss of cooling
  - Tape and taping quality
  - Allows intervention & re-work



SENTINEL™ & CLARITAS™ ARE UNIQUE TO SPTS

GaAs Dicing

- Running framed GaAs wafers on GaAs dicing process module
  - Using Si DRIE experience to produce high rate GaAs etching
- Consolidating process window
  - Considering chemistries away from traditional applications
- Integration is a factor as per Si
  - Learning from GaAs BSV being applied
- Approx 1.5x throughput c/w LASER
  - Based on ~15min LASER singulation time
  - LASER yield loss >1k ppm due to damage
  - Expect plasma to avoid this
  - Work ongoing…
- Wider process flow discussions still needed
  - Frames vs Carrier wafers; DAG vs DBG
  - This applies to other III-V materials; low volatility compounds (SiC, Glass, etc) – not suited to frames
- Paper on this topic was accepted for CS Mantech, so we will find another outlet for that later in the year



>15µm/min

Summary

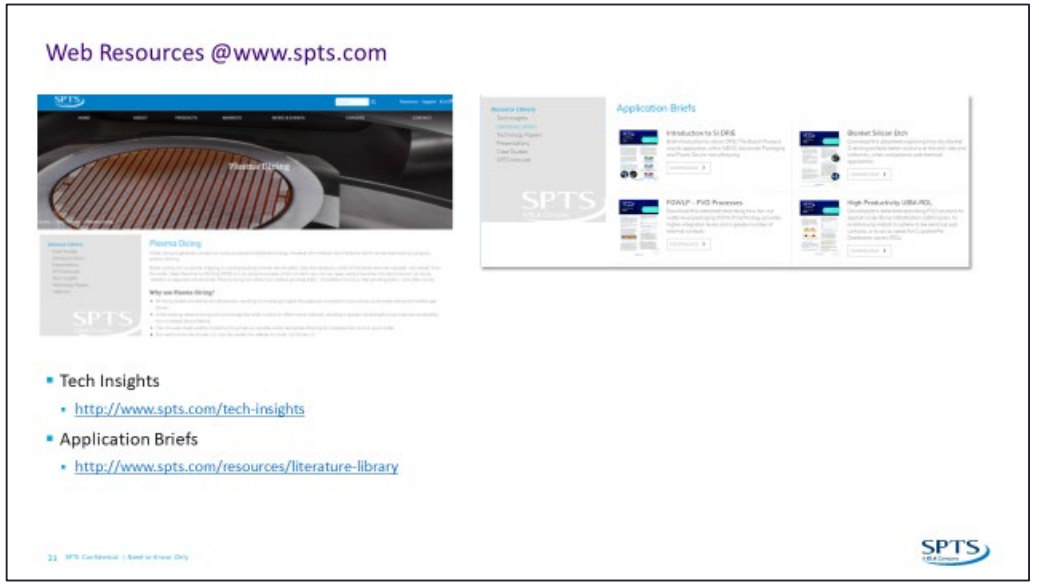
- Plasma dicing is very much here to stay
  - Benefits are clear and obvious
  - All potential barriers now have solutions; including fluorine
- Massive interest
  - Across the entire industry & markets; it is not just a die per wafer play
- Modest growth to date because Semi Industry is very conservative
  - Anxiety to move away from embedded processes and infrastructure
  - Education and experience is key to managing this
  - Plasma Dicing continues to be our largest and most subscribed demo activity
- More drivers are setting the momentum
  - SiP, Filters, HBW along with the demand for smaller die
  - GaAs
- Don’t forget plasma dicing before grind (DBG)
  - Same integration activities, wider material opportunities

For more information

- Thank you for your attention!
  - Email enquiries@spts.com
  - Keep up-to-date with SPTS @ www.spts.com

https://www.linkedin.com/company/spts-technologies-ltd

https://twitter.com/SPTS_Tech



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Questions?