Chemical Mechanical Polishing as Enabling Technology for Sub-14nm Logic Device

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- Company update
- New Era of CMP
- Sub-14nm CMP
- 450mm CMP
- Conclusions

GLOBALFOUNDRIES
Creating an Industry Leader

March
AMD spins out fab operations
ATIC acquires majority stake
GLOBALFOUNDRIES created

June
GLOBALFOUNDRIES announces new leadership

January
New York Fab delivers initial silicon first time right

February
GLOBALFOUNDRIES Launches 14nm-XM FinFET Technology

2009 | 2010 | 2011 | 2012 | 2013

TRANSFORMATION

July
Construction begins on New York Fab

September
Acquired Chartered Semiconductor

March
100% ownership by ATIC
Dresden Fab Ships 250,000th 32nm HKMG Wafer

- **Largest privately held semiconductor company**
- **Over $11B invested in Capex to date**

The First Truly Global Foundry

Malta, New York

Dresden, Germany

Singapore

- >13,000 employees
- 14 locations
- 160 customers

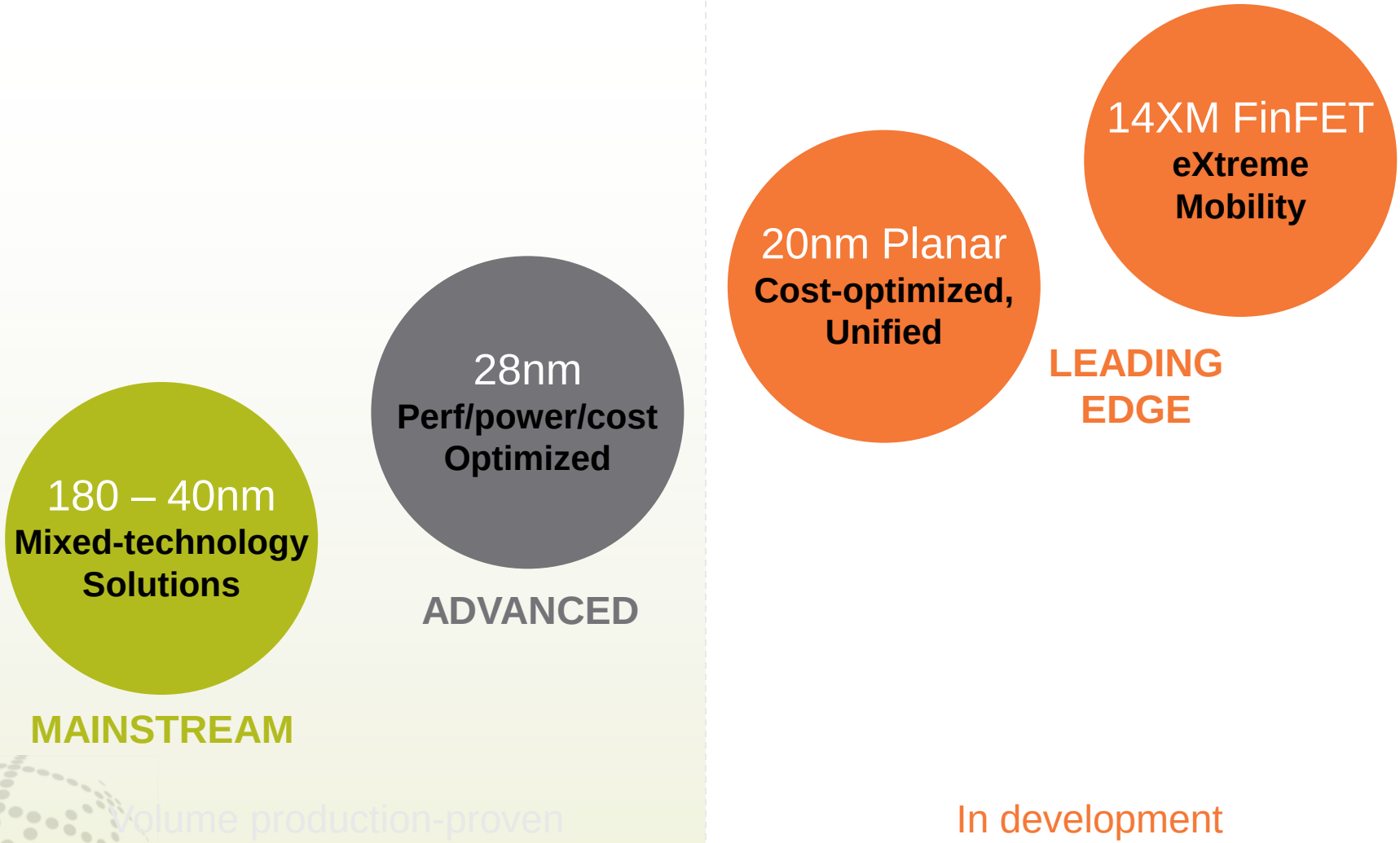
Manufacturing Centers

Regional Offices

Global Manufacturing Capacity > 4.4M Wafers/yr

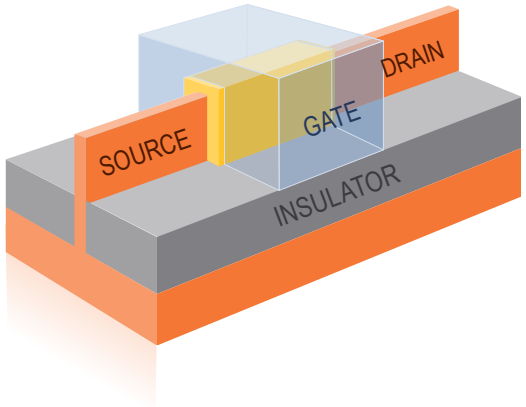
	Malta, New York	Dresden, Germany	Singapore
			
TECHNOLOGY	28nm, 20nm and ≤ 14nm	45nm to 28nm	180nm to 40nm
CAPACITY IN WAFERS/MO.	60,000	80,000	50,000 (300mm) 180,000 (200mm)
FUTURE CAPACITY	In planning	100,000	>80,000 (300mm) 180,000 (200mm)

Broad Range of Optimized Process Platforms



Leading Edge: 14XM Modular FinFET Platform
for e**X**treme **M**obility

- Targeting mobile device battery life challenge + other power-sensitive apps
  - Half the power of 28nm
  - Cost effective and manufacturable in high volumes
- Leverages 20nm planar process maturity for fastest time to volume
- Based on 10+ years of FinFET R&D
  - GF + CPA own 75% of the patents in this space
  - Builds on HKMG expertise



FinFET

- *Operates at lower Vdd*
- *Lowest off state leakage*

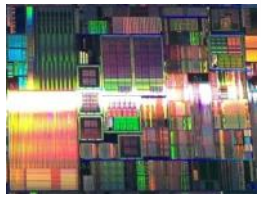
- Complete SoC solution based on deep collaboration with EDA, IP and customers
  - e.g. Synopsys, ARM, Rambus

14XM: A Range of Complete SoC Solutions

Mobile and Wireless Market Applications

Compute, Connect, Storage Market Applications

Multicore GPU Solutions



Power/perf Optimized CPU Solutions

Libraries (Standard Cells, Memories)

Mixed-signal Enablement

Processor IP

High Speed Interfaces

Full Suite PDK, Reference Flow

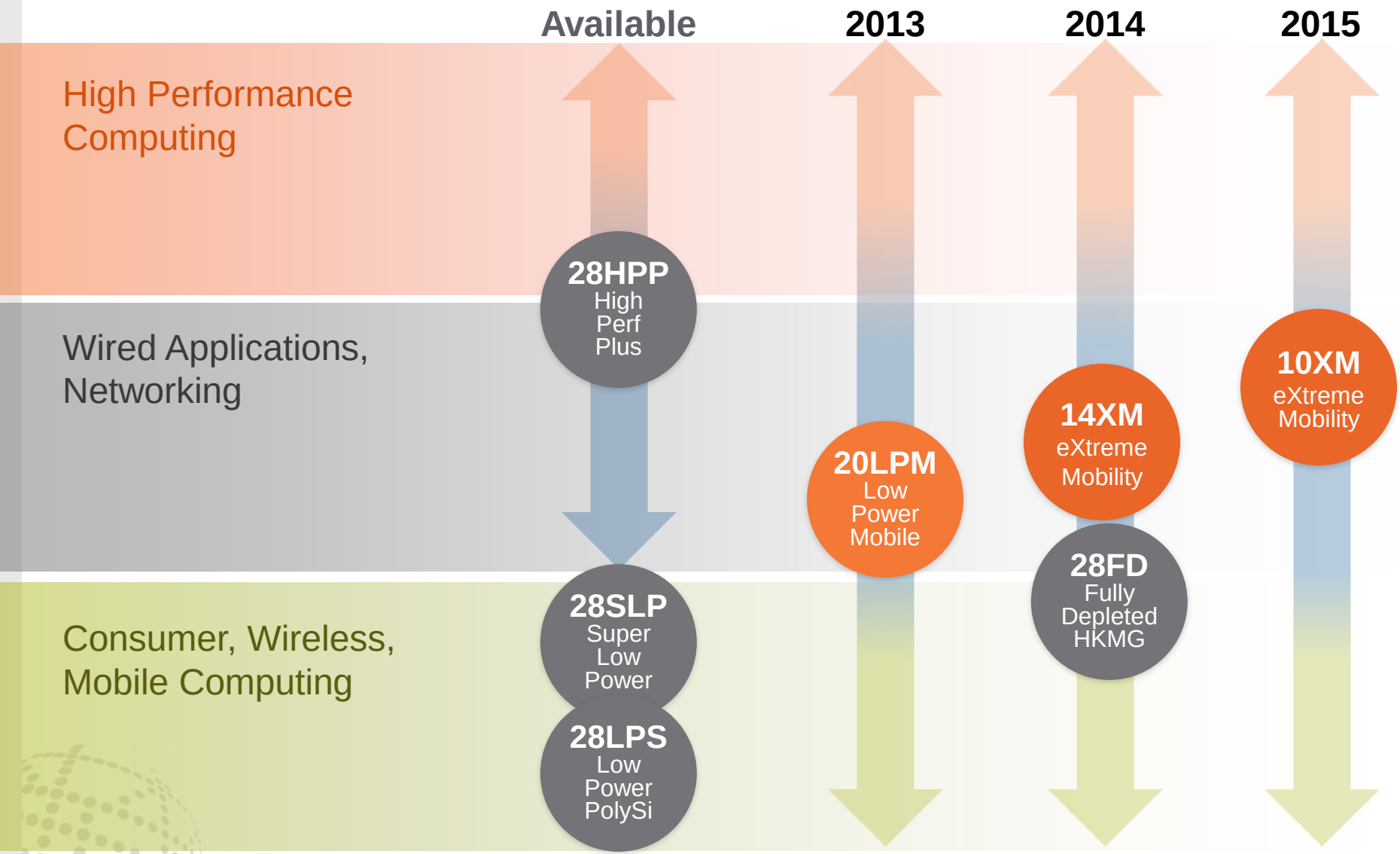
FinFET Process Technology

SoC Packaging

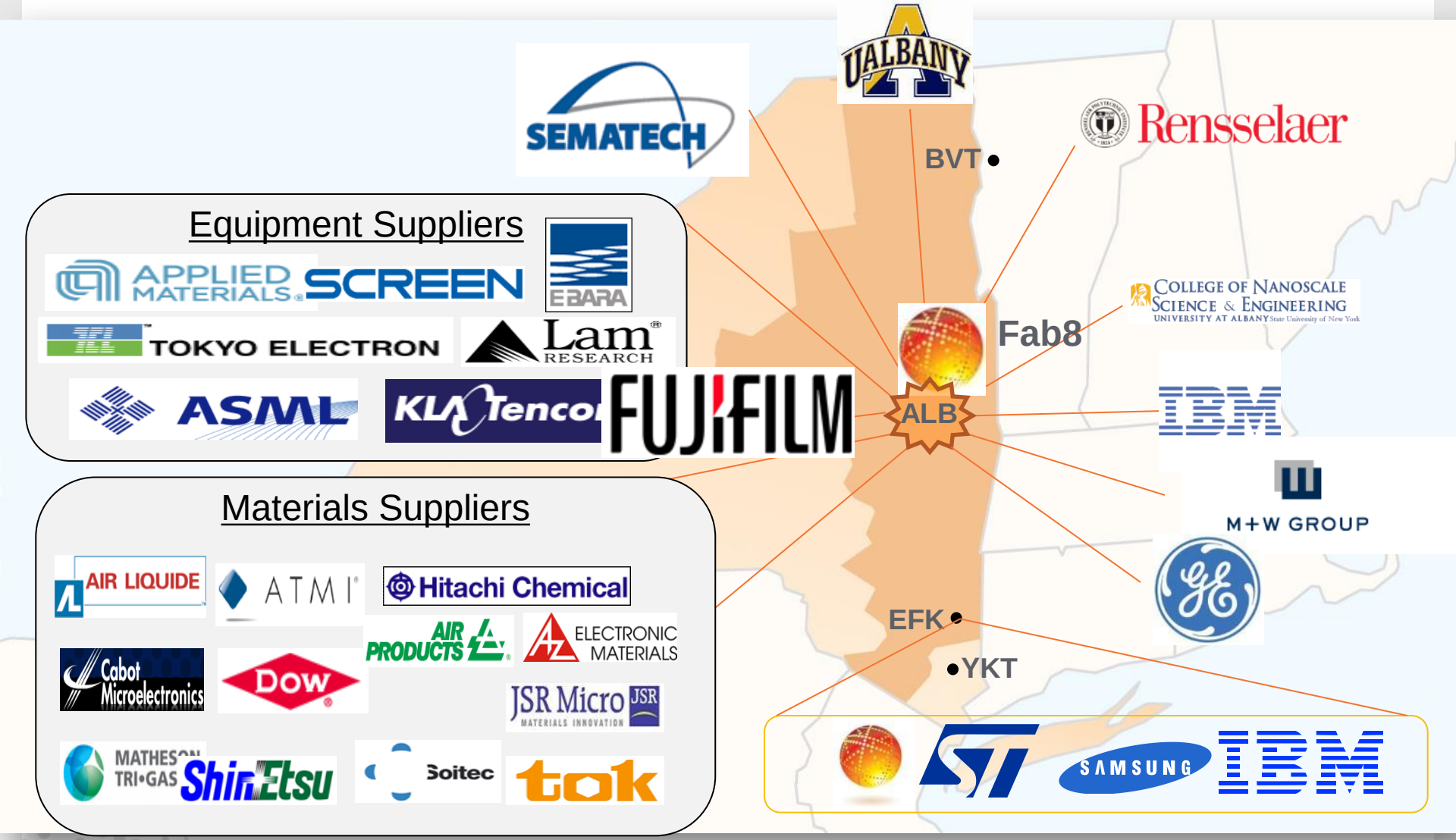
2.5D and 3D Packaging

Availability of Advanced and Leading-Edge Platforms

At the forefront of process technology

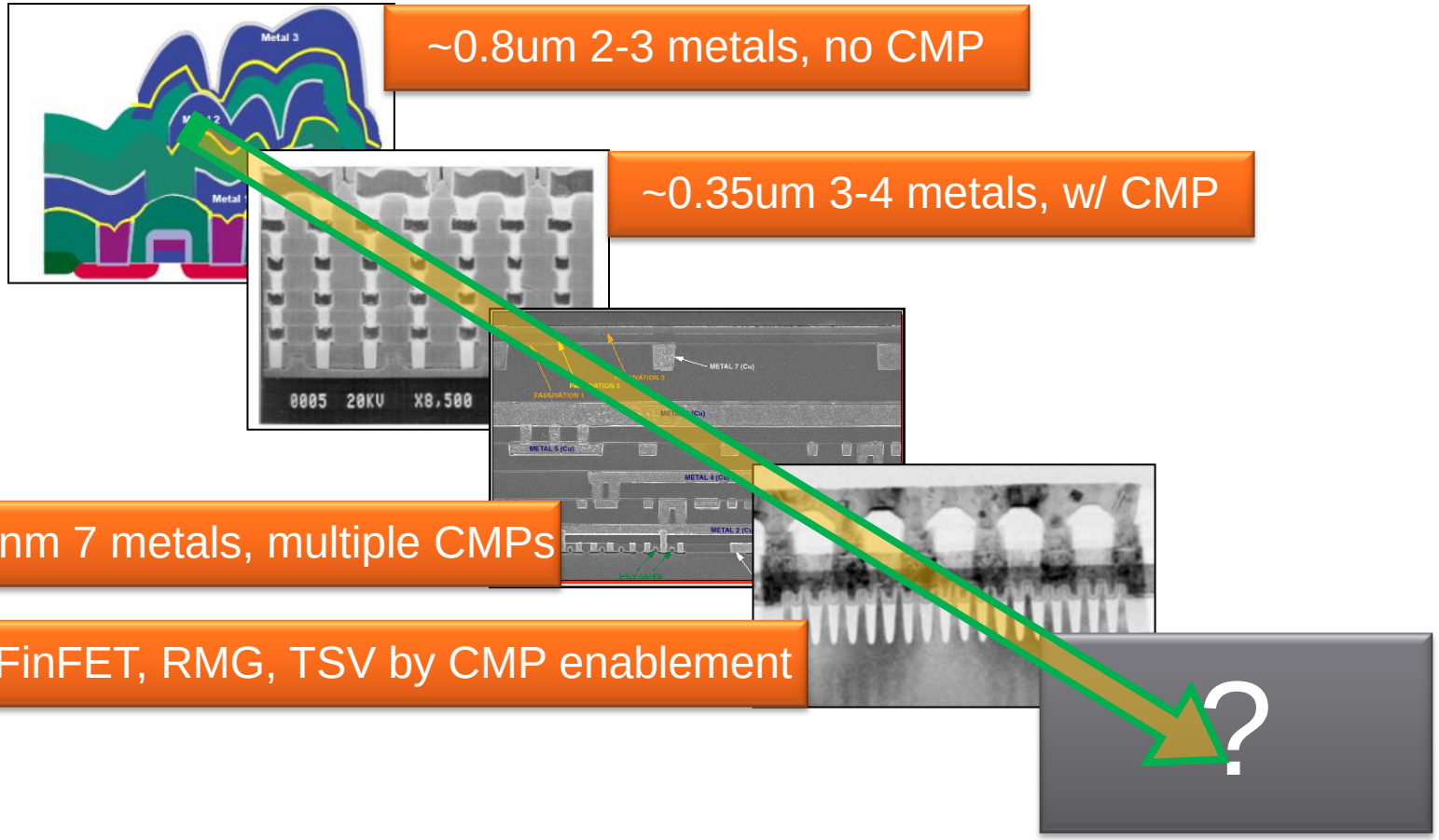


New York is the center of our Technology Ecosystem. Collaboration is a key strategy to maximize value.



New Era of CMP

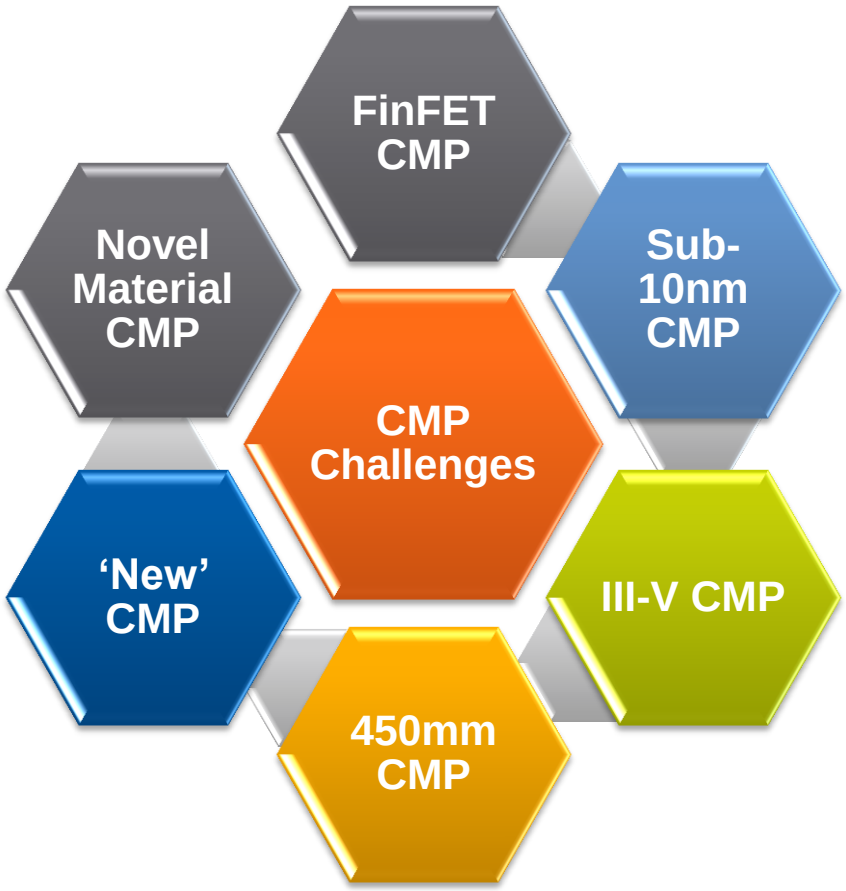
New Era of CMP applications



Non-Planar → CMP → Planar → CMP → Non-Planar

- The role of CMP is expanding from "process simplifier" to "process enabler".

CMP Challenges



- We are facing technical limitation at sub-14nm CMP technology. We must have dramatic improvement in CMP technology.
- Need to pursue technology innovation and non-conventional planarization.
- Strong collaboration among end users, tool makers, consumable suppliers, and academia is the key component to achieve this goal.

GLOBALFOUNDRIES CMP Innovation Landscape

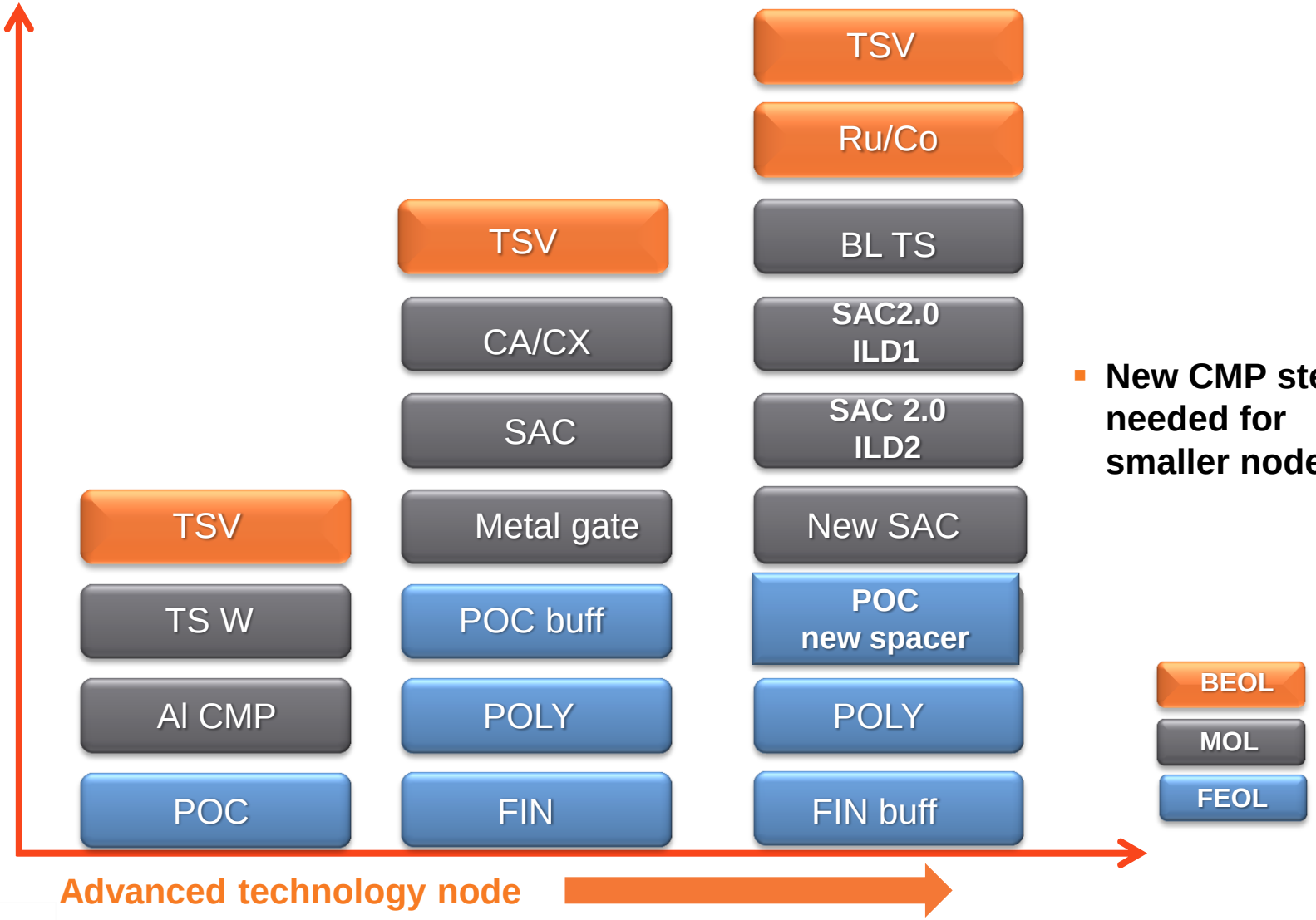
- New material research
- Sub-10nm path-finding

- New technology elements - SAC, New TS, New FINS, BEOL
- Disruptive tech
- Advanced tooling
- CMP modeling
- APC ready process and real time process control

- Tool matching
- Fault detection control
- Cost reduction initiatives

Research, development, and manufacturing collaboratively work for CMP excellence at GLOBALFOUNDRIES.

GLOBALFOUNDRIES CMP process roadmap

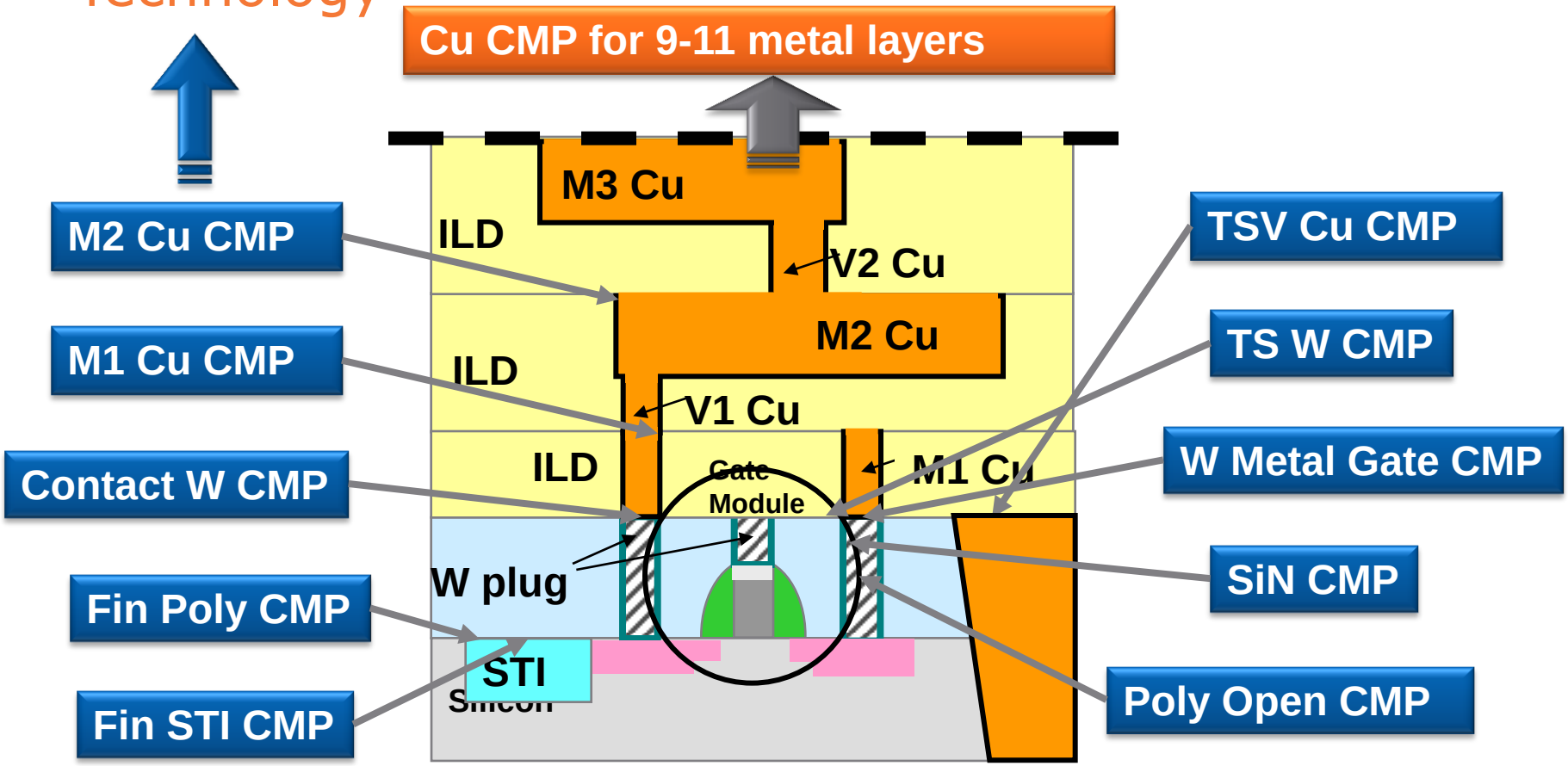


- **New CMP steps needed for smaller nodes**

More FEOL/MOL CMP applications needed for future node.

Sub-14nm CMP

CMP Process Steps for Sub-14nm Logic Technology



- In modern logic device fabrication, the number of CMP steps required in FEOL/BEOL integration reaches up to 18-20.
- More CMP applications are in need for FEOL/MOL integration.
- Metal gate CMP is the most challenging step for sub-14nm CMP processes.

Major CMP challenges in sub-14nm node

- Scratching/particle reduction
  - Silica vs. Ceria abrasive
  - Hydrophobic surface
  - 'Hardpad like' softpad
- Tighter WIW/WTW/LTL control
  - Stringent process control requirement (less than 40~60A)
  - Automatic process control by in-situ endpoint technology, real-time profile control, and integrated metrology.
- 'Tunable' selectivity
  - Extremely high selectivity vs. non-selectivity

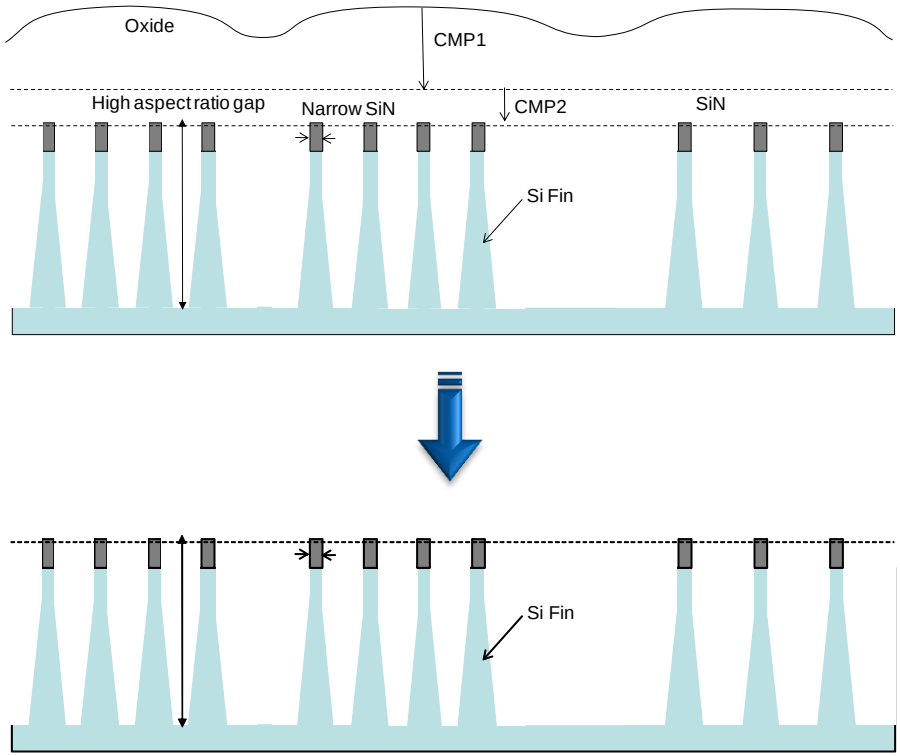
Major CMP challenges in sub-14nm node

- No more in-film stop process without advanced process control!
  - Stop-on-planarization slurry
  - 'Multiple' process control technologies for WIW/WTW/LTL control
- 'Zero' dishing/erosion
  - Extremely high selectivity vs. non-selectivity
  - 'Harder' pad for better topography and planarization efficiency
- Disruptive 'non-CMP' technology
- Advanced post CMP cleaning capability

CMP steps in FinFET Integration Scheme

- FinFET STI CMP
- *FinFET Polysilicon CMP
- Poly open CMP (POC) in RMG at FinFET
- Metal gate W CMP in RMG at FinFET
- *Silicon nitride capping CMP in RMG at FinFET
- Contact W CMP in MOL at FinFET
  - *New additional CMP steps at FinFET integration

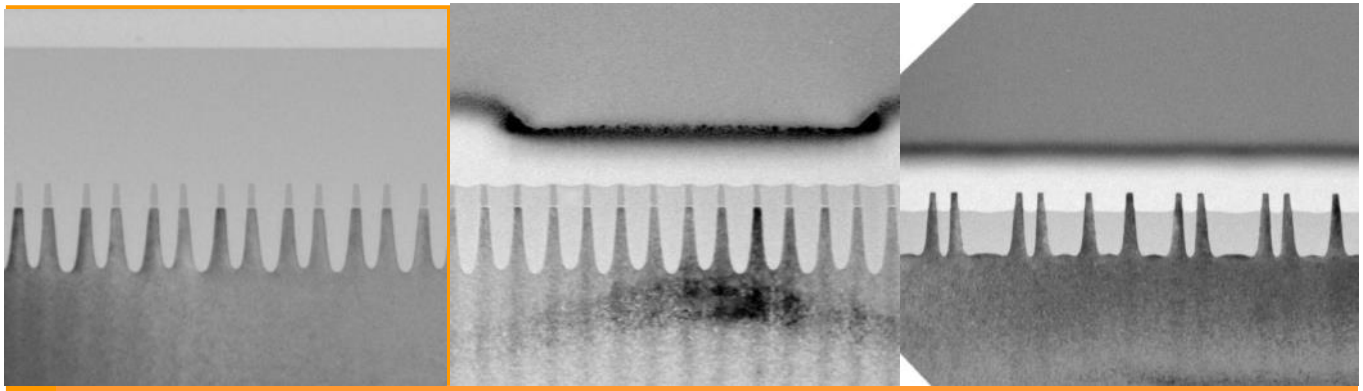
FinFET STI CMP



- CMP step removes bulk oxide and stops on nitride with minimum nitride erosion and oxide dishing.
- High selective slurry is required to eliminate nitride loss.
- Topography control at post STI CMP is important to minimize any within-in chip oxide thickness variation.

Key Challenges in FinFET STI CMP

Post oxide dep	Post STI CMP	Post etch back



SiN erosion/loss is typically less than 50A.

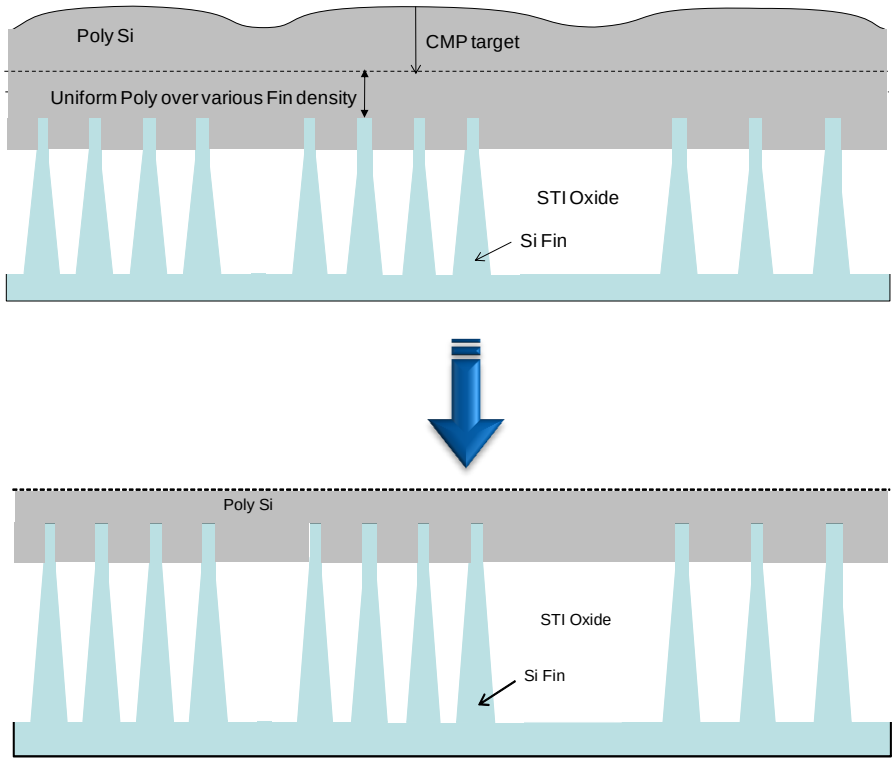
Step height control

Step height in STI CMP became significantly critical due to Fin/RMG integration scheme. Step height or ‘oxide dishing’ carried over from STI to Fin/RMG module will impact on yield and device performance at RMG module. Tight process control for WIWNU/WTWNU/WIDNU at STI CMP is a critical prerequisite for successful Fin/RMG module. Uniform pattern density/dummy fill design is necessary to minimize oxide dishing.

Minimum/uniform nitride loss

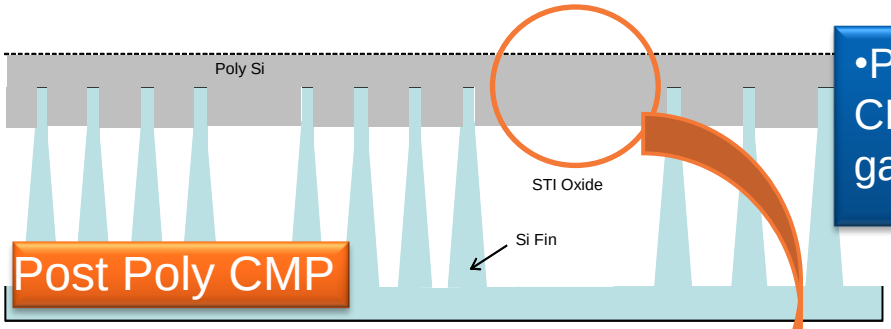
Minimum nitride loss is challenging due to narrower and thinner active nitride. Uniform nitride loss across Fin density is critical to ensure overall within die uniformity.

FinFET Poly CMP

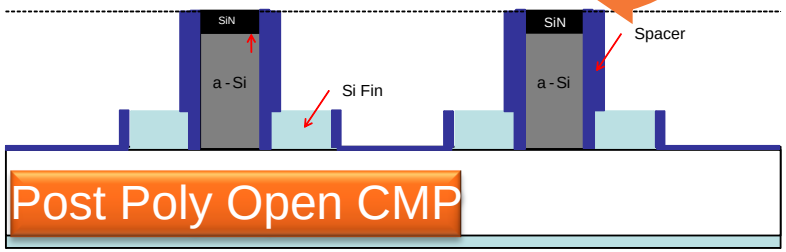


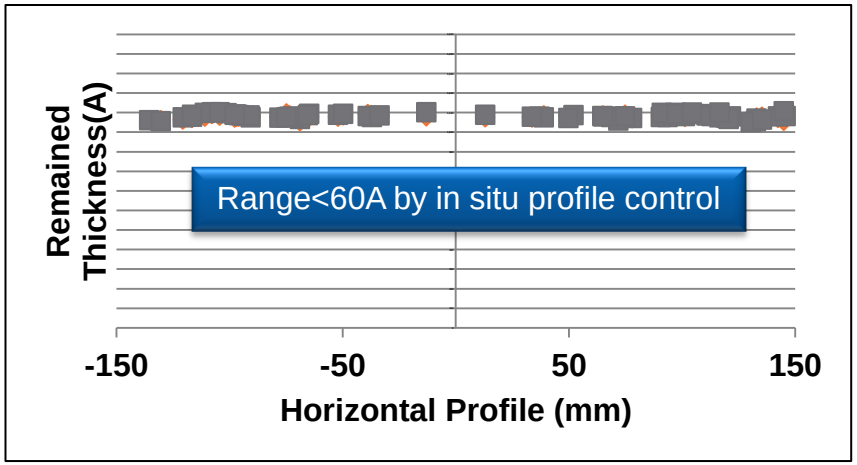
- After nitride strip, oxide recess, and poly deposition, poly CMP is required to planarize polysilicon on top of Fin and STI oxide.
- A good planarization efficiency is needed in poly CMP to planarize polysilicon with minimum poly removal amount and to ensure uniform poly thickness across different Fin density.

WIW/WTW control in FinFET Poly CMP



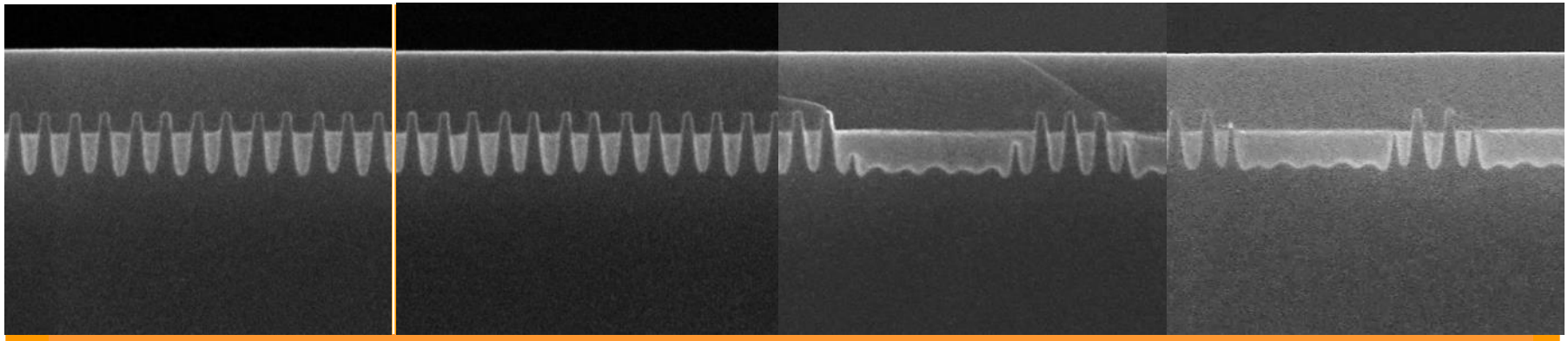
•Poly thickness uniformity after poly CMP directly transferred to dummy poly gate height uniformity.





- Any remaining poly non-uniformity impacts on device performance and yield.
- WIWNU/WTWNU is the challenge in FinFET poly CMP due to stop in film process and can't leverage material selectivity.
- Need to use advanced CMP technology including automatic process control and in-situ automatic profile control to meet this tight spec.

Key Challenges in FinFET Poly CMP



Within-chip poly thickness variation is typically less than 60A.

Planarization

Due to thin incoming polysilicon film, superior planarization is required to eliminate any gate CD variation by litho due to surface non-planarity.

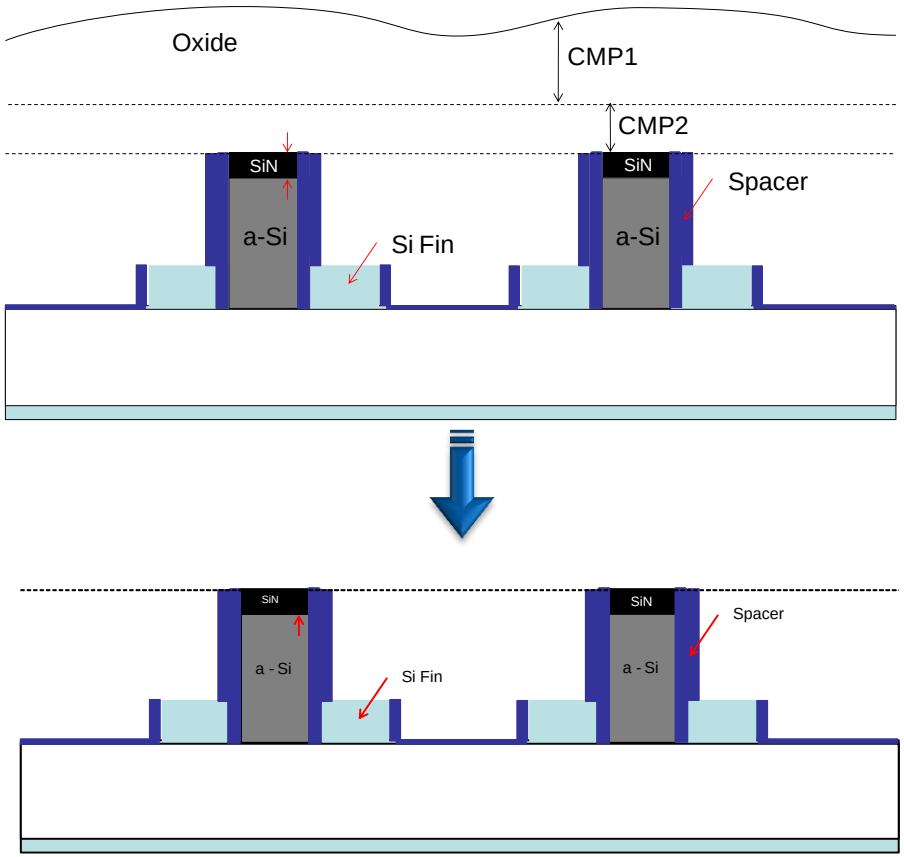
Within-wafer-uniformity control

Thin polysilicon thickness target needs tight wafer-scale uniformity control of polysilicon film.

Endpoint

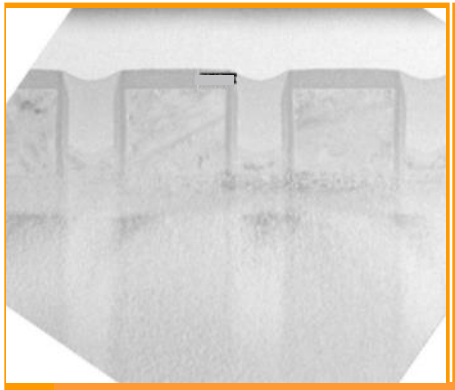
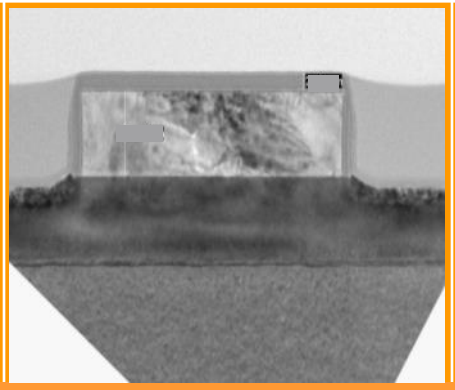
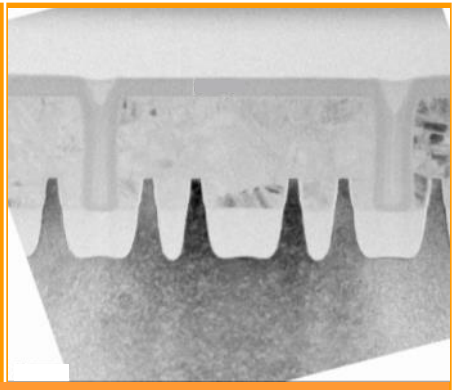
Accurate process endpoint is a must to control the thin polysilicon thickness target. Due to opaque optical property of the polysilicon film, advanced endpoint system (such as short wavelength spectroscopy) is essential.

FinFET RMG Poly Open CMP (POC)



- Height of dummy poly gate is controlled by previous poly CMP.
- CMP1 step removes bulk oxide and planarize surface prior to stop on nitride step.
- CMP2 step stops on nitride with minimum cap nitride erosion. High selective slurry is required to eliminate nitride loss and to maintain good gate height.

Key Challenges in Poly Open CMP (POC)

Macro1	Macro2	Macro3
		

SiN erosion/loss is typically less than 50A.

Extremely high selective slurry process

Extremely high-selective slurry process is the key to control the process with minimum nitride loss and required to ensure tight final gate height at both long and short channels. . Uniform pattern density/dummy fill design is necessary.

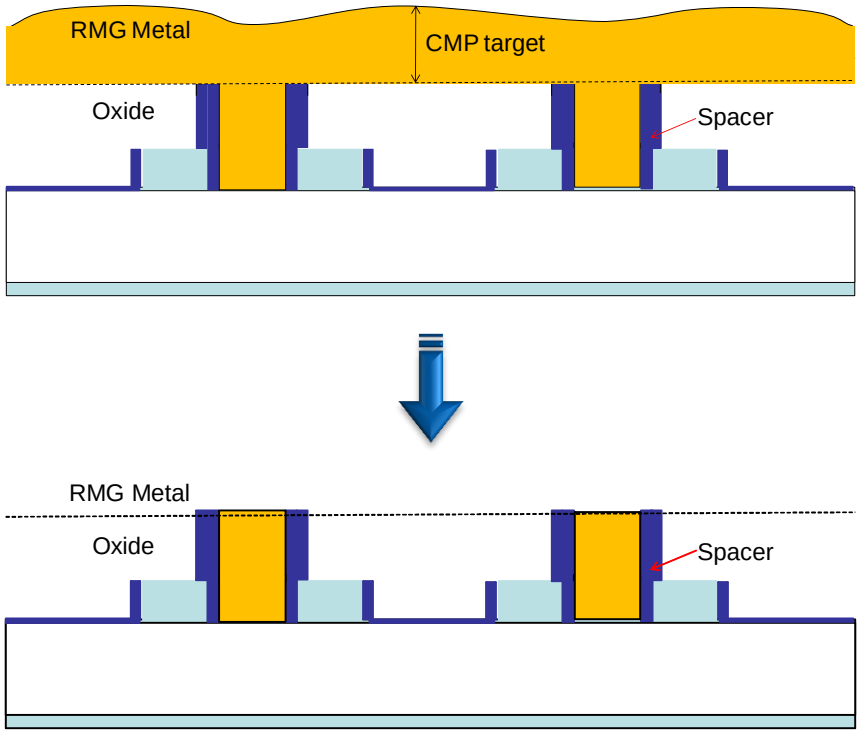
Gate height control

Gate height in RMG module became significantly critical since it will impact on yield and device performance at RMG module. Uniform pattern density/dummy fill design is necessary to minimize nitride loss and to ensure uniform gate.

Minimum/uniform nitride loss

Minimum nitride loss is challenging due to narrower and thinner active nitride. Uniform nitride loss across Fin density is critical to ensure overall within die uniformity.

FinFET RMG W Gate CMP



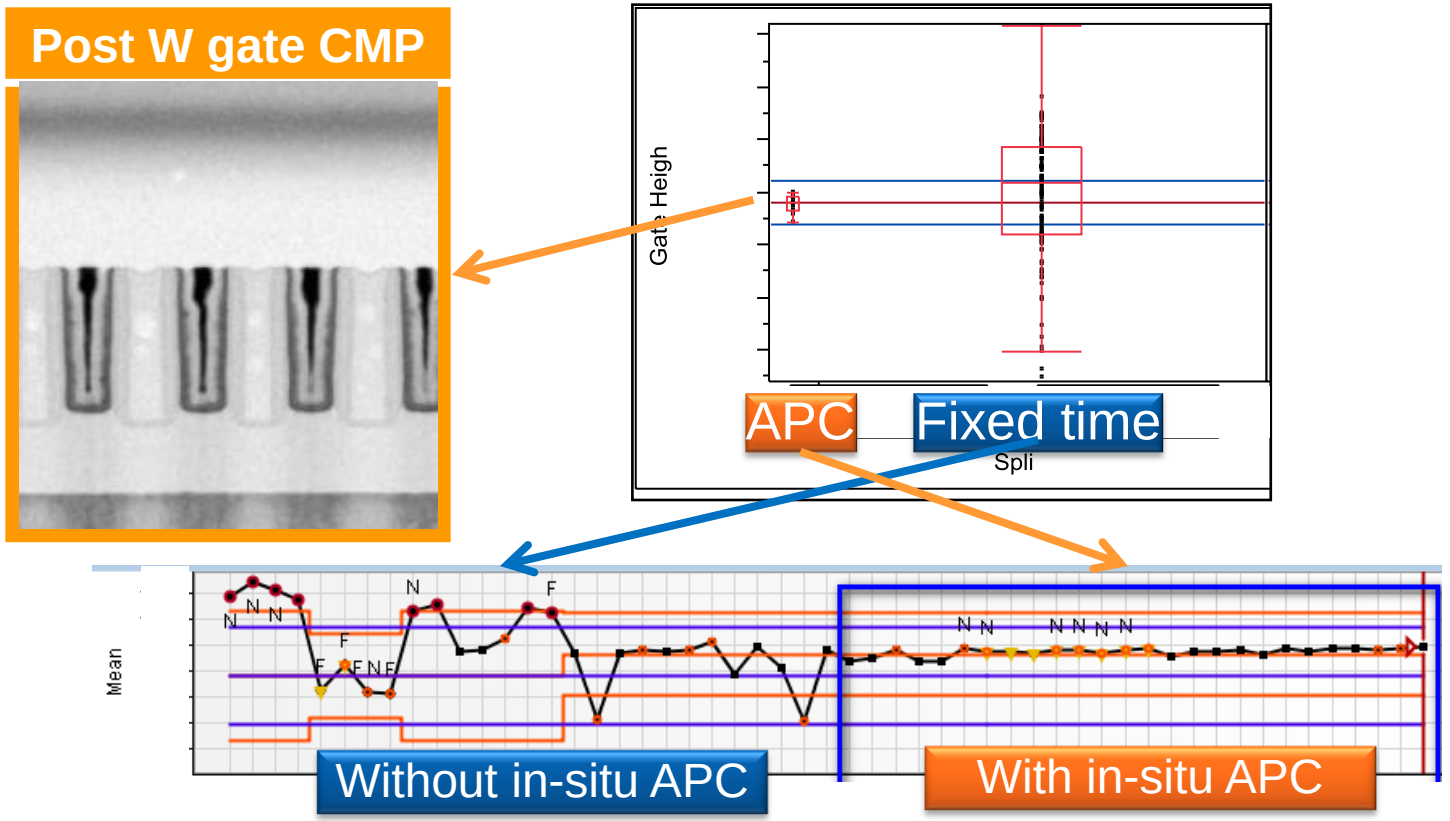
- Metal gate W CMP is the most critical step in RMG module since this step determines the final gate height .
- Metal gate W CMP process itself is very similar to regular Cu damascene process.
- Oxide loss margin is very narrow due to close proximity to Fin and tight gate height control.

W gate CMP is the most critical CMP step in 14nm FinFET CMP processes.

Key Challenges in FinFET RMG W CMP

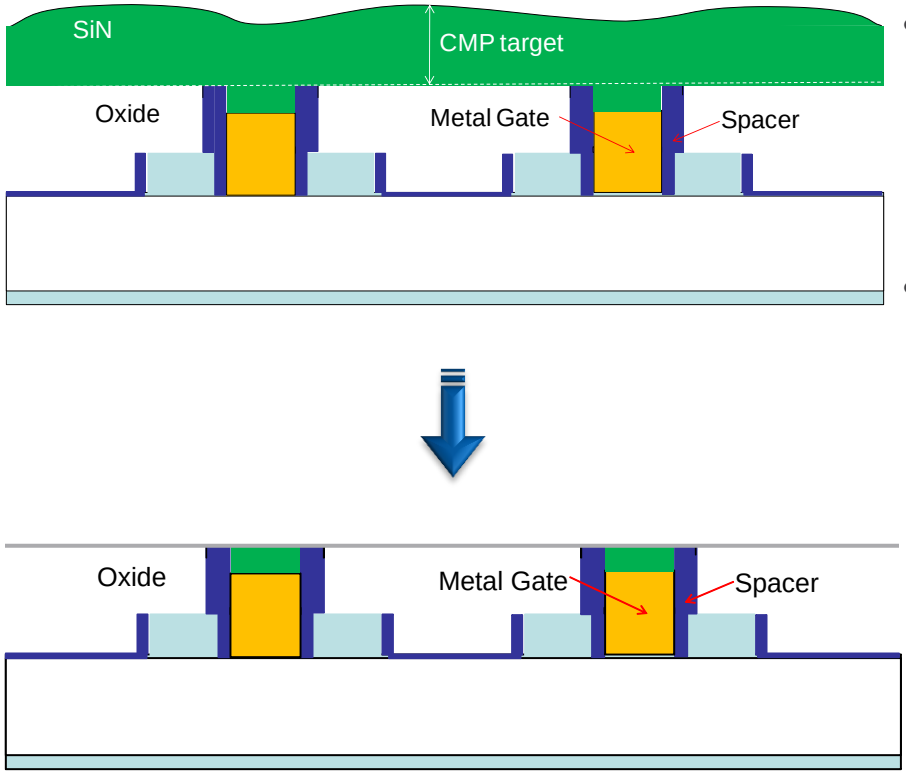
- Extremely high selective slurry process
  - Extremely high-selective slurry process is the key to control the process with minimum oxide loss and required to ensure tight final gate height at both long and short channels. . Uniform pattern density/dummy fill design is necessary.
- Gate height control
  - Gate height in RMG module became significantly critical since it will impact on yield and device performance at RMG module. Uniform pattern density/dummy fill design is necessary to minimize nitride loss and to ensure uniform gate.
- Zero dishing or protrusion
  - ‘Zero dishing or protrusion’ metal gate CMP process is a must to eliminate impact on device performance.
- Defect-free CMP
  - ‘Any defect’ will directly impact on yield and device performance. Defectivity needs to be eliminated in metal gate CMP step..

WTW control in W gate CMP



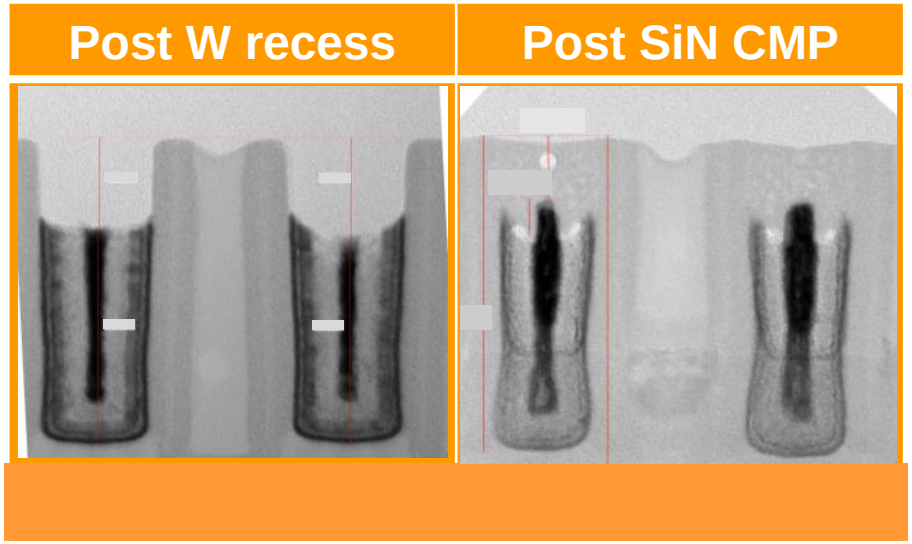
- Due to process variability, CMP needs to ‘accommodate’ incoming variation to achieve tight W gate height control.
- More than 8x improvement observed at W gate height control with ‘real time’ automatic process control process.
- R-APC is enabled using on-board metrology.

FinFET Self Aligned Contact (SAC) SiN Cap CMP



- After metal gate recess and SiN deposition, CMP needs to remove SiN to create SiN cap on top of metal gate.
- Highly selective slurry against oxide is required to minimize oxide loss and wafer-scale non-uniformity.

Key Challenges in SiN CMP



Extremely high selective slurry process

Extremely high-selective slurry process is the key to control the process with minimum oxide loss.

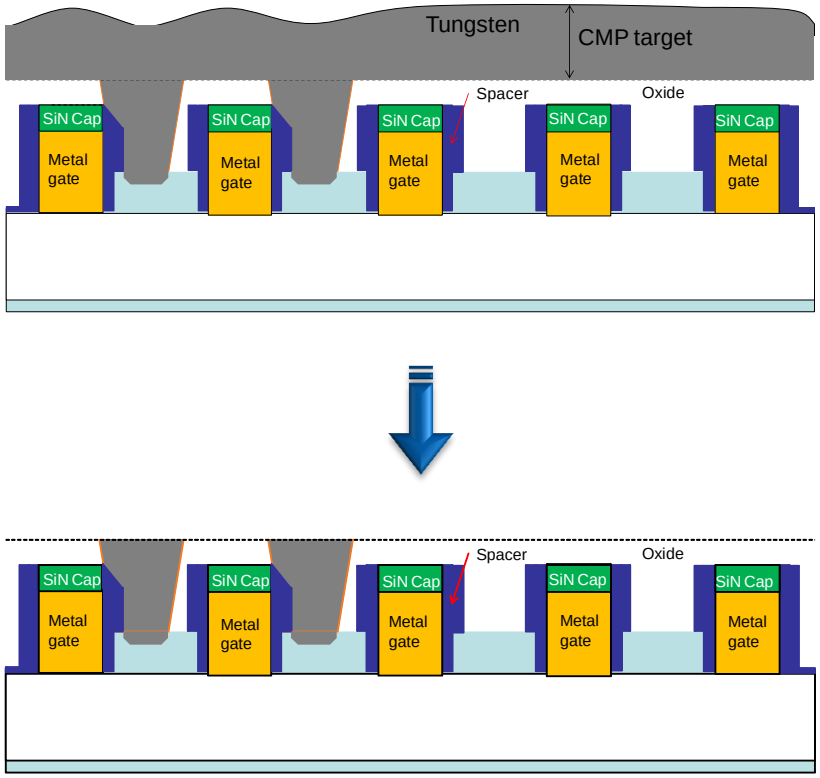
Endpoint control

Endpoint can be tricky due to ‘less-unique’ boundary between oxide and nitride.

Void-free SiN fill

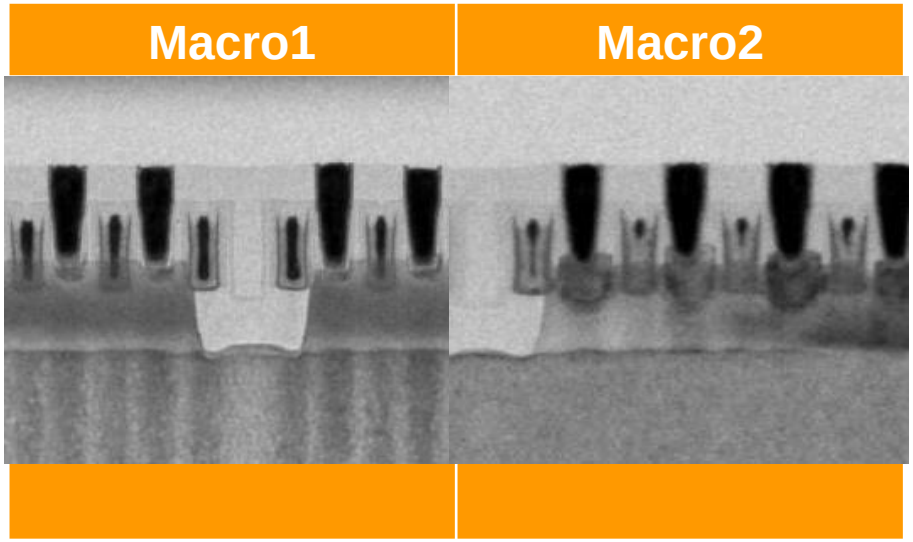
Due to minimum gate length and high aspect ratio, void-free SiN fill can be challenging.

Contact W CMP in MOL at FinFET



- Contact W CMP is very similar to one used in previous node.
- Oxide loss allowance is very minimum and less room to recover for any W contact erosion.

Key Challenges in W contact CMP



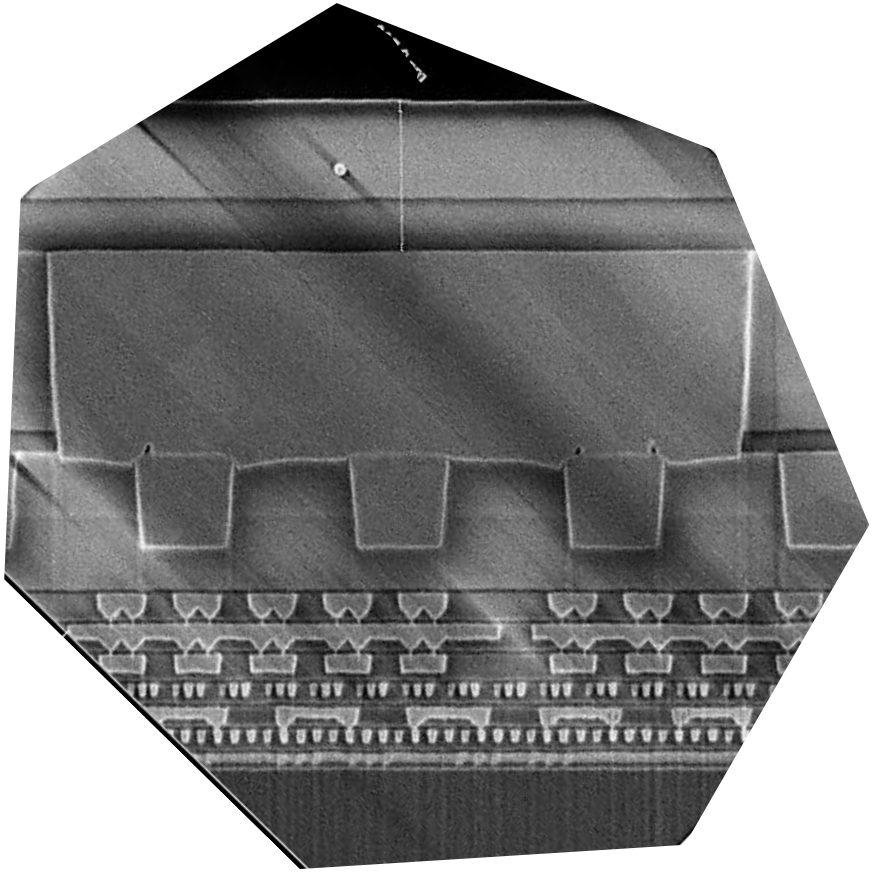
Minimum topography

W CMP for contact module requires minimum within-die uniformity and topography to prevent ‘residue’ in the following contact level. Protrusion or recess of W contact impacts on device yield and performance due to CA-M1 open or resistivity variation
Extremely high-selective slurry process is the key to control the process with minimum oxide loss.

Defectivity

Advanced buffing slurry and cleaning chemistry are needed to prevent galvanic corrosion in tungsten. The modulation of removal rate selectivity became the key parameter to control W gate topology..

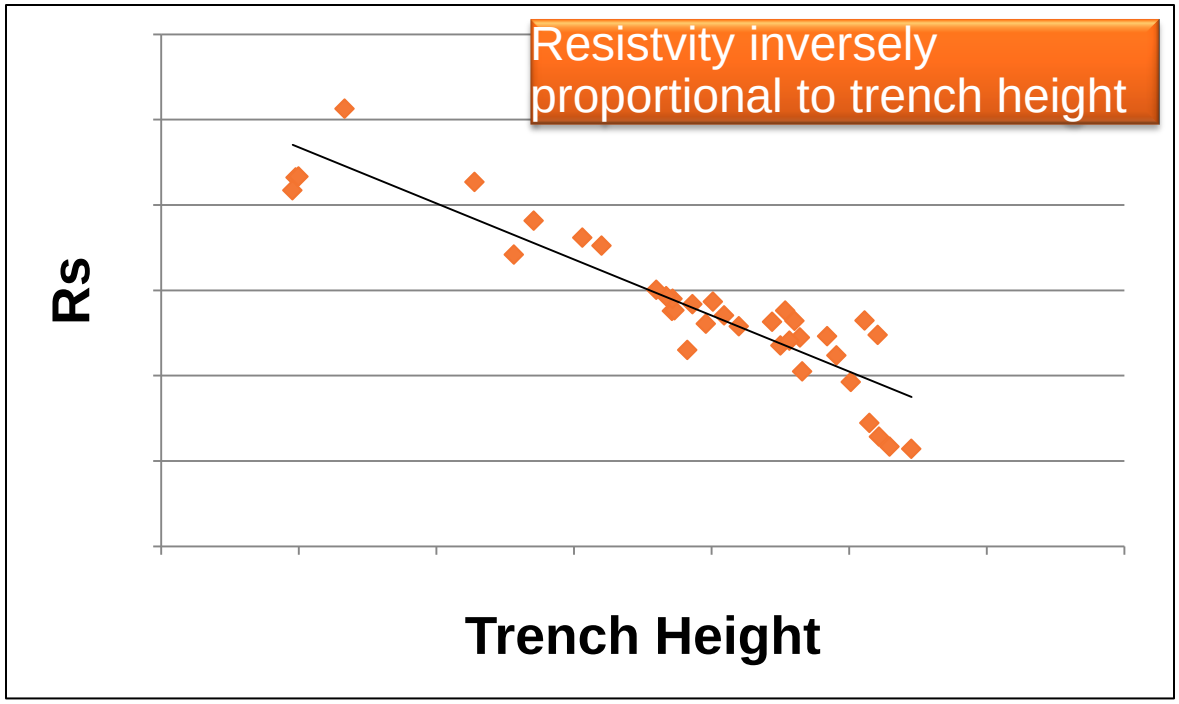
Cu CMP at 14nm

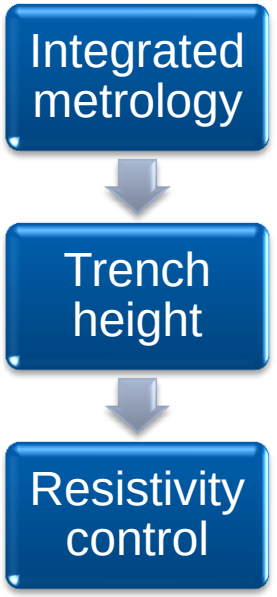


- Defectivity control is one of the major challenges at 14nm Cu CMP. Scratch and residue/particle are two major defect modes.
- Due to tight resistivity control, in-situ APC is the critical requirement at Cu CMP.
- Reliability requirement enforces proper choice of post Cu CMP cleaning chemistry.

Eight Cu metal layers have been demonstrated at 14nm FinFET technology.

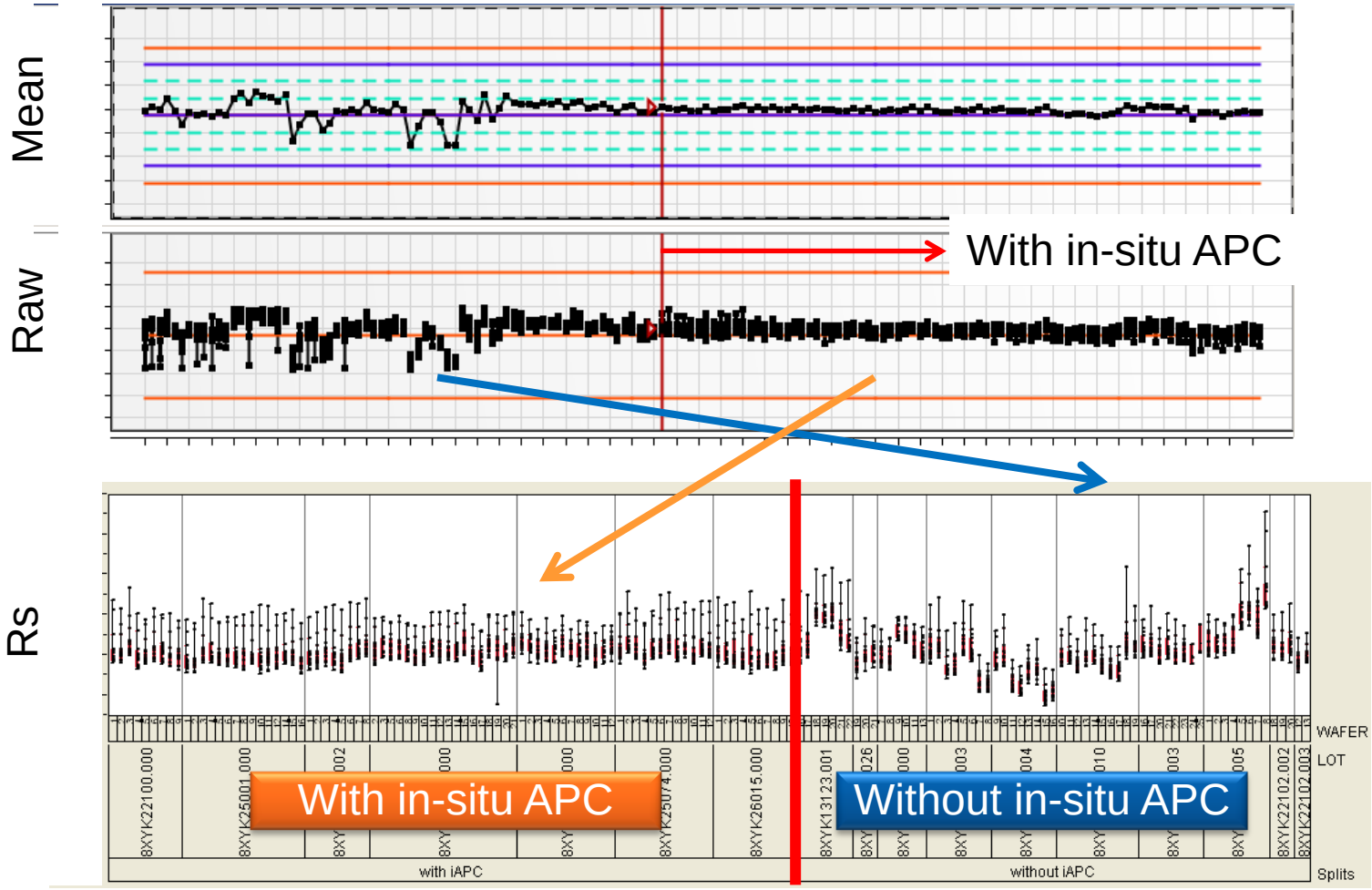
In-situ APC at 14nm Cu CMP





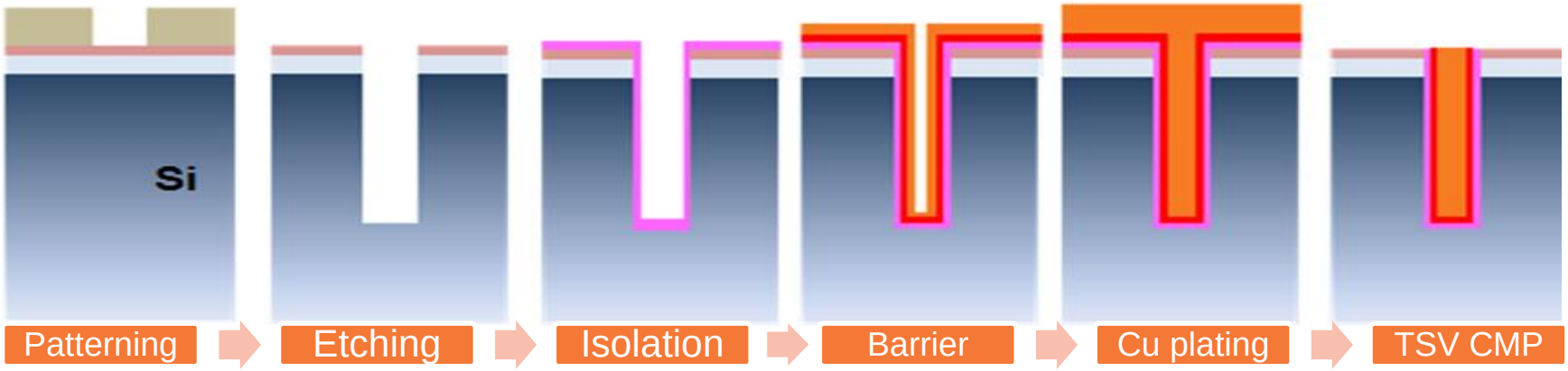
- By using in-situ APC, trench height is automatically controlled and, thus, consistent Cu resistivity can be maintained.

In-situ APC at 14nm Cu CMP



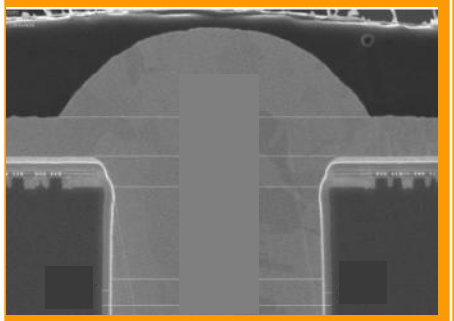
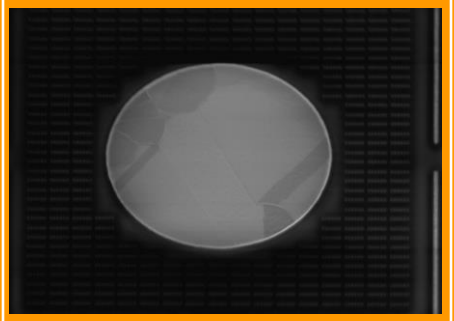
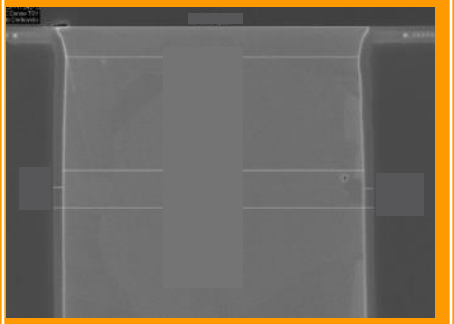
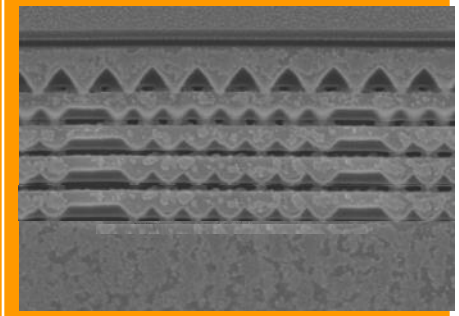
- WTW/LTL resistivity control has been improved by 80% due to in-situ automatic process control.

TSV (Through Silicon Via) Cu CMP



- **TSV Cu CMP** process is required for through silicon via (TSV) applications. Thicker Cu overburden and barrier, and higher oxide loss spec requires high removal rate Cu and barrier/oxide slurries. 'Harder' pad is required to minimize Cu dishing as less than 100A.

Key Challenges in TSV Cu CMP

Post Plating	Post CMP	Post CMP	Post CMP
			

Minimum topography

High Cu dishing after TSV Cu CMP may cause degradation at BEOL integration. Less than 100A topography is required and can be achieved by proper selectivity at Cu and barrier removal processes. It is critical to maintain uniform contact cap near TSV and field area.

Process control

Due to incoming variation, automatic process control is needed to ensure consistent post TSV Cu CMP ILD thickness control.

Sub-10nm CMP Challenges

- Fin formation continues to be one of the major challenges due to thinner SiN stop layer.
- Tunable selectivity is required to provide complete non-selectivity with extreme selectivity against the third material such as oxide, nitride, and polysilicon.
- Evolution of non-Si Fins make CMP more challenging as advanced slurries with new noble materials such as Ge or III-V materials.
- Zero-recess or protrusion for any metal CMP is essential to minimize any impact on device performance.
- Integrated metrology continues to be the ‘must’ technology enablement to play as ‘eyes at CMP tool’ to look at every single wafer for precise process control.

Sub-10nm CMP Challenges

- In-situ endpoint system must be improved to differentiate subtle thickness change in sub-10nm CMP.
- Non-Cu metal can replace Cu for BEOL metallization and corrosion-free metal CMP will be a challenge.
- Dramatic improvement is required for post CMP cleaning module due to stringent defectivity requirement. Single wafer clean process can replace post CMP cleaning module.
- Non-conventional ‘disruptive’ planarization method will be implemented as ‘complimentary’ process to CMP.

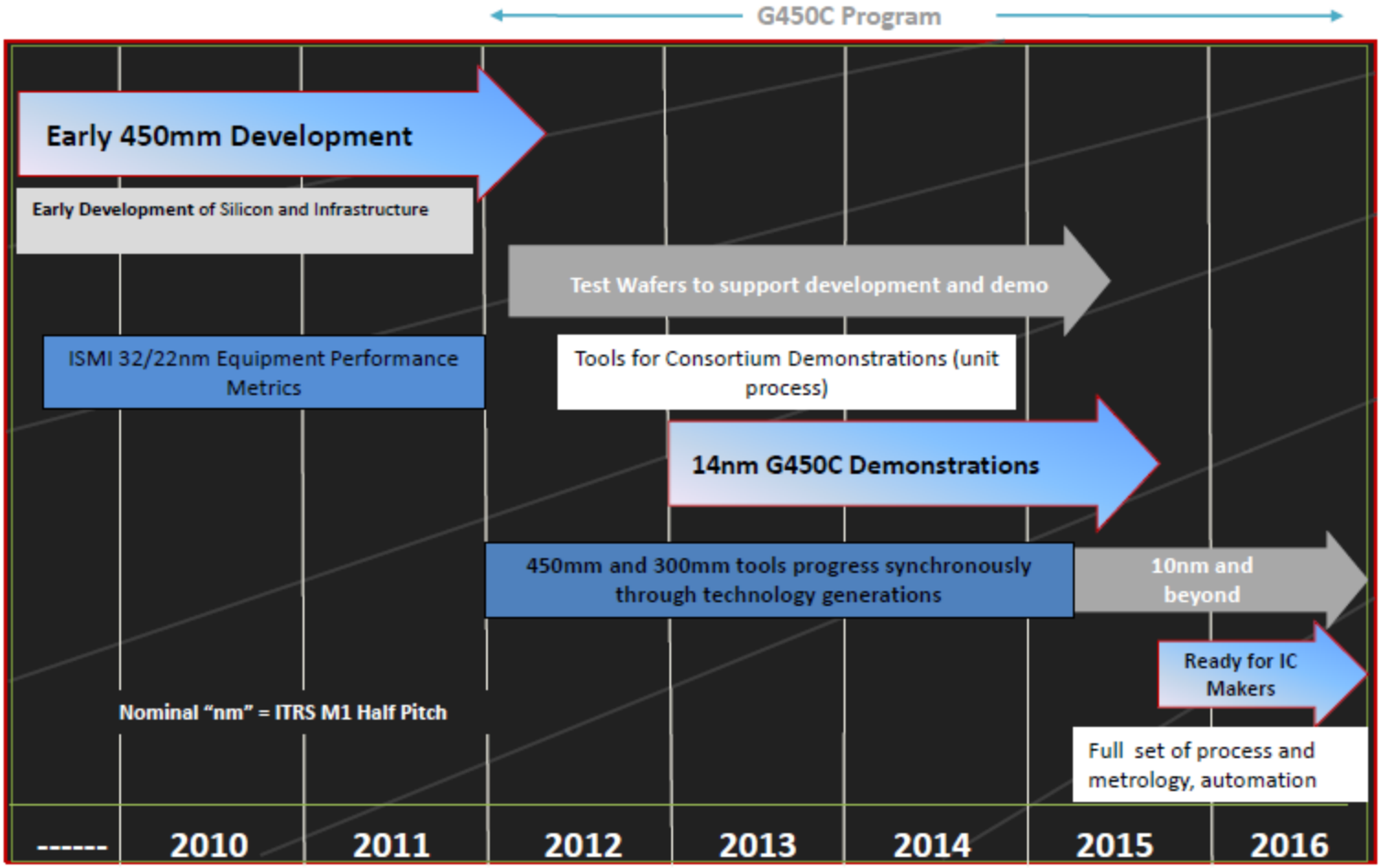
450mm CMP

450mm Program at GLOBALFOUNDRIES

- GLOBALFOUNDRIES is part of G450C program at CNSE.

From: http://www.g450c.org/default.aspx

Development and Technology Intercept Targets



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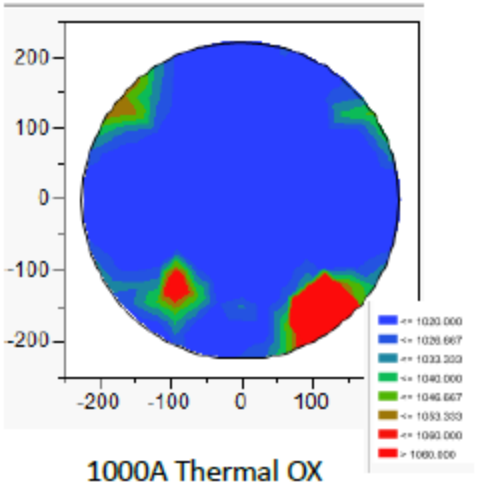
From: http://www.g450c.org/default.aspx

Thermal/CMP/Cleans Module Data

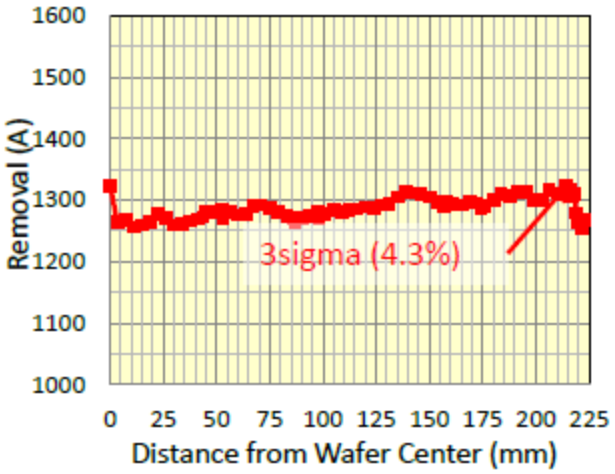
- Demonstrate Thermal OX capability →U%(3s)1.97%(EPM<2%)
- Demonstrate OX CMP capability →U%(3s)4.3% (EPM<4%)
- Demonstrate Cleans capability →U%(3s) 1.1% (EPM<0.5%)

Thermal OX



1000A Thermal OX

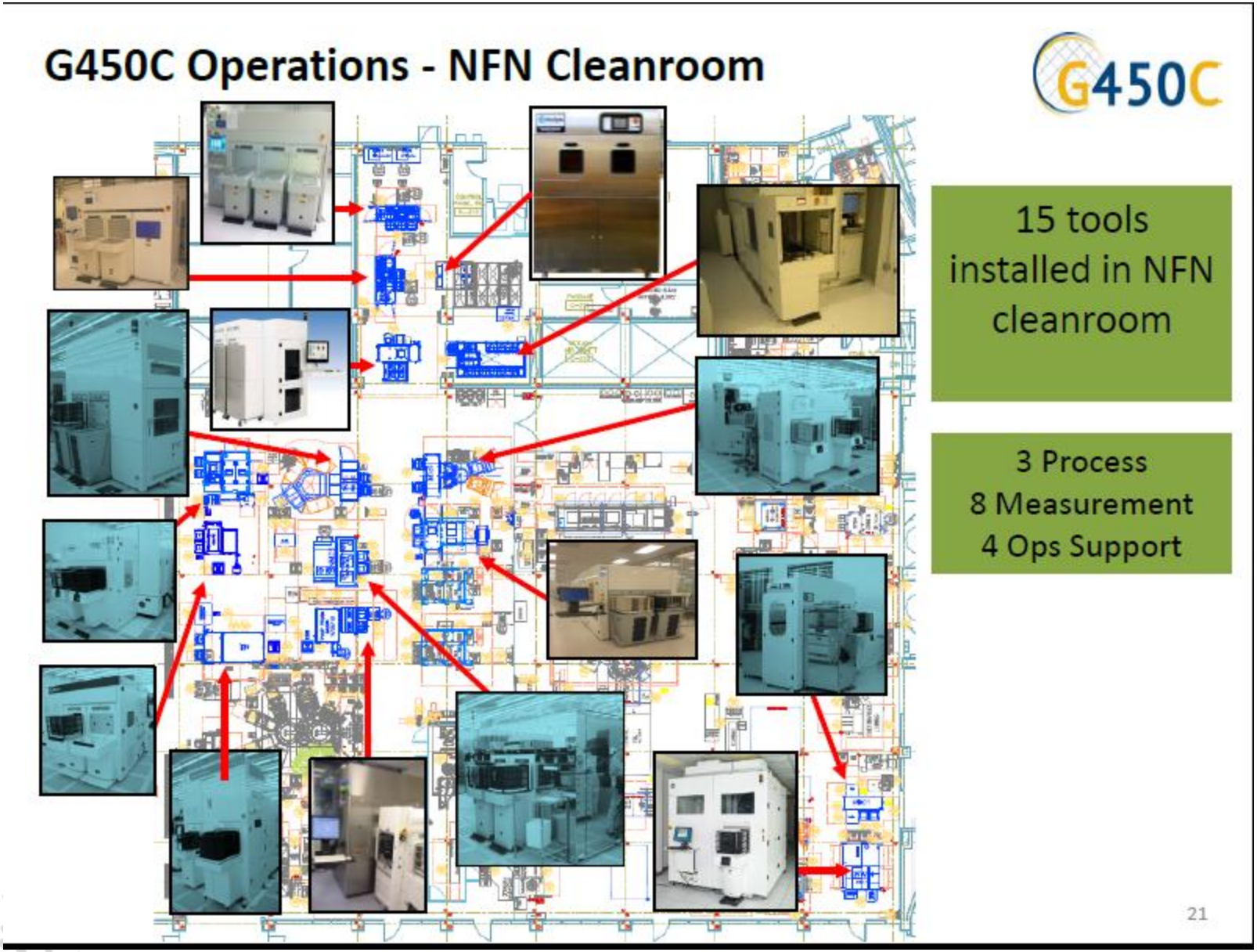
OX CMP



Cleans

DHF (50:1) Etch rate

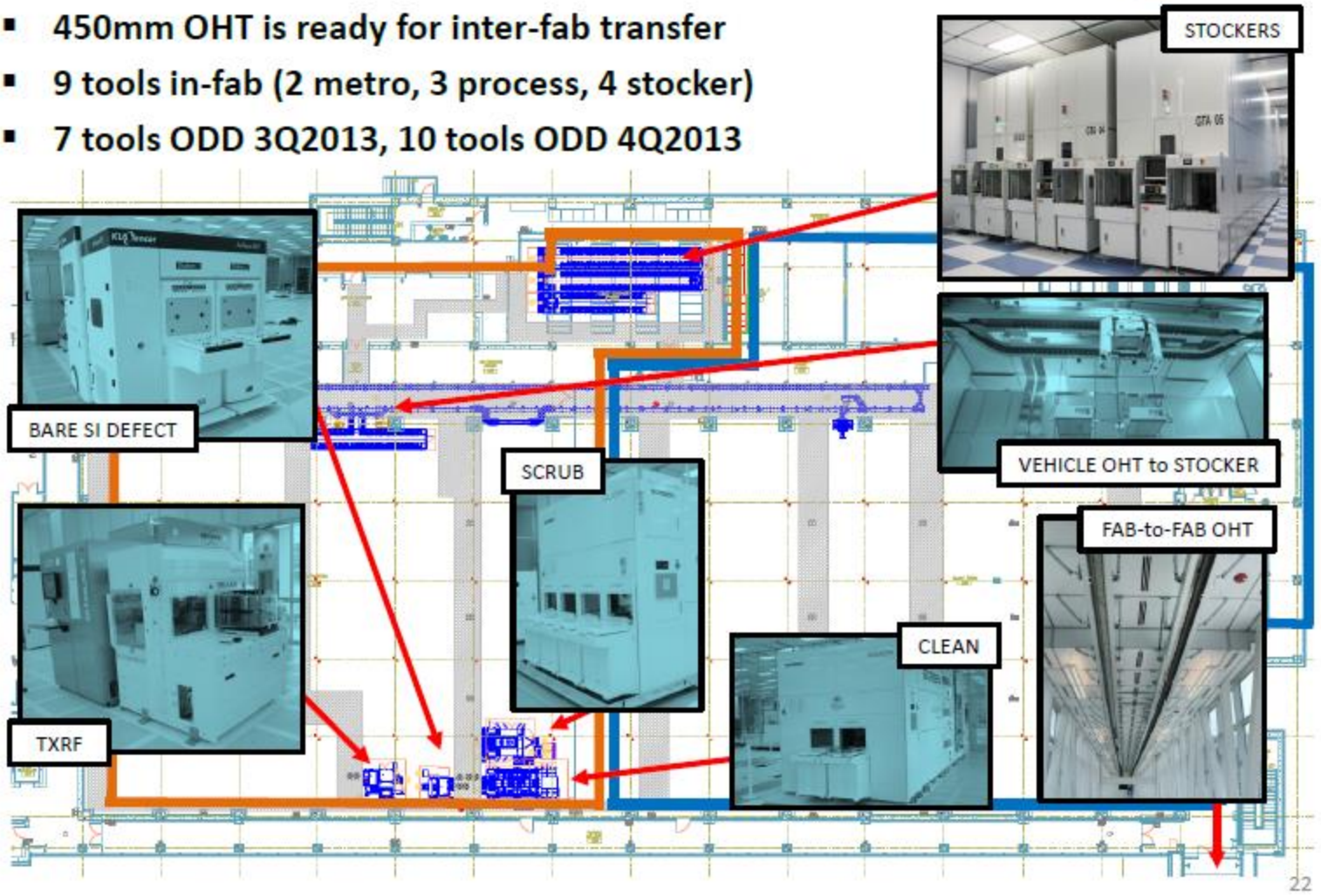
From: http://www.g450c.org/default.aspx



From: http://www.g450c.org/default.aspx

G450C Operations - NFX Cleanroom

- 450mm OHT is ready for inter-fab transfer
- 9 tools in-fab (2 metro, 3 process, 4 stocker)
- 7 tools ODD 3Q2013, 10 tools ODD 4Q2013



From: http://www.g450c.org/default.aspx

Summary

- G450C has launched with full industry momentum
- Significant progress towards the 450 mm transition is continuing in all areas of the supply chain
- Suppliers are developing the 450mm tool set with ~ 10 tools per quarter being delivered to G450C
- Significant progress has been made in wafer quality and wafer reclaim is almost ready
- Automation and carriers are working
- Suppliers are cooperating on key initiatives
- Global collaboration is picking up steam

From: http://www.g450c.org/default.aspx

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Conclusions

- We are in a historical moment to determine ‘the destiny of CMP’ in sub-14nm technology. CMP can continue to be a enabling technology, or role of CMP can be minimized by having non-conventional planarization technology.
- We must have dramatic improvement in CMP technology. To maintain the competitiveness of CMP, the following requirements need to be achieved;
  - WIW/WTW process control
    - No more in-film stop process without advanced process control!
  - Defect improvement
  - Cost reduction
  - Superior planarization efficiency
  - Tunable ‘smart’ slurry (highly selective, vs. non-selective)
  - Versatile endpoint technology for novel materials
- Strong collaboration among end users, tool manufacturers, consumable suppliers, and academia is the key to meet this challenge.

Thank you

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